



带LDO模式,过压和过流保护IC 以及锂电池充电器前端保护IC

说明

CS5801T 是一个高度集成的电路,旨在保护锂离子电池免受充电电路故障的影响。该IC 可持续监视输入电压、输入电流和电池电压。输入过压保护通过关断内部开关立即停止为充电电路供电。输入保护可将系统电流限制为用户可编程的值,如果过流情况仍存在,则在一个消隐周期之后关断导通元件。此外,该IC 还会监控自身的芯片温度,并在过热时切断电源。该IC 可由一个处理器控制并且可为主机提供关于故障条件的状态信息。CS5801T提供纤小的DFN2X2_8L的封装,可以为客户节省可观的PCB面积,其额定的工作温度范围为-40°C至85°C。

特性

- 针对三个变量提供保护:
 - 输入过压、快速响应 $< 1\mu\text{s}$
 - 带有电流限制的用户可编程过流
 - 电池过压
- 30V 最大输入电压
- 支持高达1.5A 的输入电流
- 防止由电流瞬变造成的错误触发
- 电池防反接保护
- 过热保护
- 输入使能
- 状态指示-故障状态
- 5.15V LDO模式电压调节

封装

- DFN2X2_8L

应用

- 智能手机
- MP3 播放器
- 低功耗手持设备
- 蓝牙耳机等蓝牙设备

典型应用电路

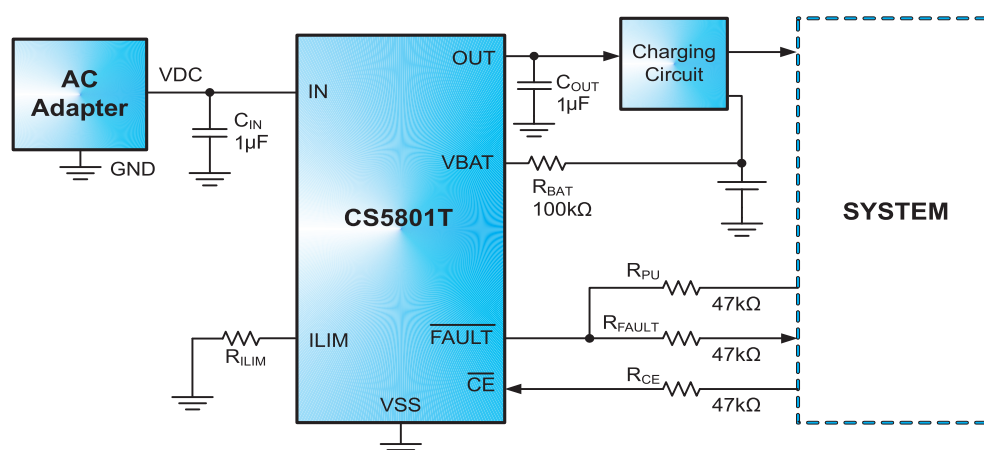


Figure a. 典型应用电路



OVERVOLTAGE AND OVERCURRENT PROTECTION IC AND Li+ CHARGER FRONT-END PROTECTION IC WITH LDO MODE

DESCRIPTION

The CS5801T is highly integrated circuits designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage, the input current, and the battery voltage. The output acts as a linear regulator. The output is regulated to $V_{O(REG)}$ for inputs between $V_{O(REG)}$ and the overvoltage threshold. If an input overvoltage condition occurs, the IC immediately removes power from the charging circuit by turning off an internal switch. In the case of an overcurrent condition, it limits the system current at the threshold value, and if the overcurrent persists, switches the pass element OFF after a blanking period. Additionally, the IC also monitors its own die temperature and switches off if it exceeds 140°C. The input overcurrent threshold is user-programmable.

The IC can be controlled by a processor and also provides status information about fault conditions to the host.

FEATURES

- Provides Protection for Three Variables:
 - Input Overvoltage, with Rapid Response in $< 1\mu s$
 - User-Programmable Overcurrent with Current Limiting
 - Battery Overvoltage
- 30V Maximum Input Voltage
- Supports up to 1.5A Input Current
- battery anti - access protection
- Robust Against False Triggering Due to Current Transients
- Thermal Shutdown
- Enable Input
- Status Indication – Fault Condition
- 5.1V LDO Mode Voltage Regulation

APPLICATIONS

- Mobile Phones and Smart Phones PDAs
- MP3 Players
- Low-Power Handheld Devices
- Bluetooth™ Headsets

Package

- DFN2X2_8L

TYPICAL APPLICATION CIRCUIT

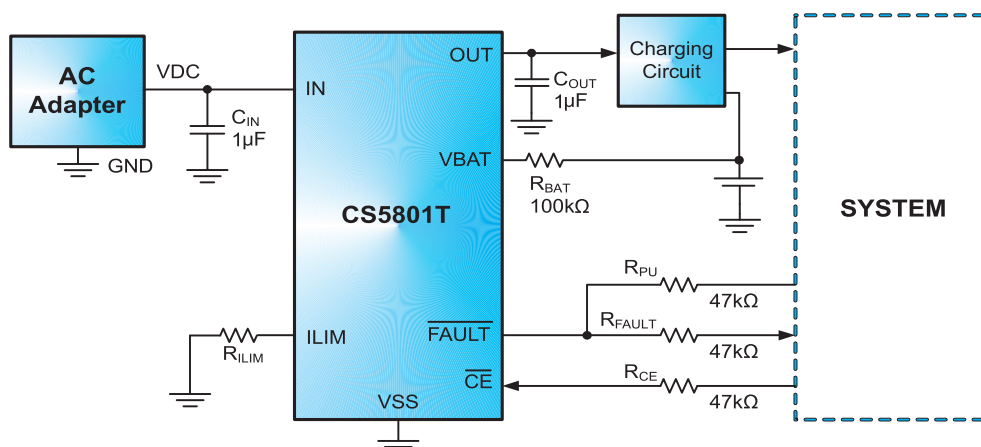
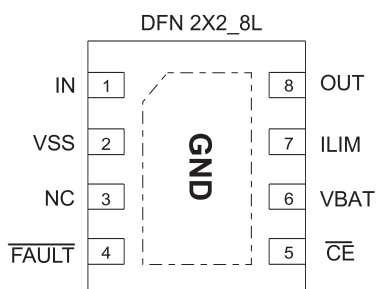


Figure a. Typical Application Circuit

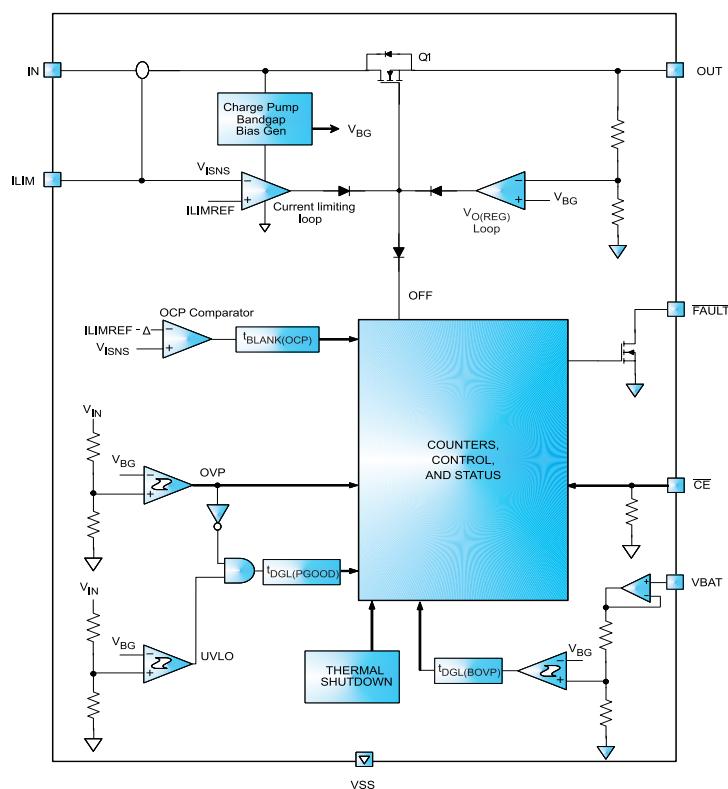
PIN CONFIGURATION (TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	PIN		
IN	1	I	Input power. Connect IN to the external DC supply. Bypass IN to VSS with a 1μF ceramic capacitor (minimum).
VSS	2	–	Ground terminal
NC	3		This pin may have internal circuits used for test purposes. Do not make any external connection to this pin for normal operation.
FAULT	4	O	Open-drain, device status output. $\overline{\text{FAULT}}$ = Low indicates that the input FET Q1 is off due to input overvoltage, input overcurrent, battery overvoltage, or thermal shutdown. $\overline{\text{FAULT}}$ is high impedance during normal operation. Connect a pullup resistor from FAULT to the desired logic level voltage rail.
$\overline{\text{CE}}$	5	I	Chip enable active low input. Connect $\overline{\text{CE}}$ = High to disable the IC and turn the input FET off. Connect $\overline{\text{CE}}$ = low for normal operation. $\overline{\text{CE}}$ is internally pulled down.
VBAT	6	I	Battery voltage sense input. Connect to the battery pack positive terminal through a resistor.
ILIM	7	I/O	Input overcurrent threshold programming. Connect a resistor from ILIM to VSS to set the overcurrent threshold.
OUT	8	O	Output terminal to the charging system. Connect OUT to the external load circuitry. Bypass OUT to VSS with a 1μF ceramic capacitor (minimum).
Thermal PAD		–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. The VSS pin must be connected to ground at all times.

Simplified Block Diagram(Figure 1)





ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	PIN	VALUE	UNIT
V _I	Input voltage	IN (with respect to VSS)	−0.3 to 30	V
		OUT (with respect to VSS)	−0.3 to 7	
		ILIM, FAULT, CE, VBAT (with respect to VSS)	−0.3 to 7	
I _I	Input current	IN	2	A
I _O	Output current	OUT	2	A
	Output sink current	FAULT	15	mA
ESD	Withstand Voltage	All (Human Body)	2000	V
		All (Machine)	200	V
		All (Charge Device)	500	V
		IN (with IN bypassed to the VSS with a 1-μF low-ESR ceramic capacitor)	15 (Air Discharge) 8 (Contact)	kV
T _J	Junction temperature		−40 to 150	°C
T _{stg}	Storage temperature		−65 to 150	°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{IN}	Input voltage range	3.3	30	V
I _{IN}	Input current, IN pin		1.5	A
I _{OUT}	Output current, OUT pin		1.5	A
R _(ILIM)	OCP Programming resistor	15	90	kΩ
T _J	Junction temperature	−40	125	°C

Order Information

Device	Package	Making	Reel Size	Tape Width	Quantity
CS5801T	DFN2X2_8L	5801D XXXX	7"	8mm	3000



ELECTRICAL CHARACTERISTICS

over junction temperature range -40°C to 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IN						
UVLO	Undervoltage lock-out, input power detected threshold	$\overline{\text{CE}} = \text{Low}$, V_{IN} increasing from 0V to 3V	2.6	2.7	2.8	V
$V_{\text{hys}}(\text{UVLO})$	Hysteresis on UVLO	$\overline{\text{CE}} = \text{Low}$, V_{IN} decreasing from 3V to 0V	160	200	240	mV
$t_{\text{DGL}}(\text{PGOOD})$	Deglitch time, input power detected status	$\overline{\text{CE}} = \text{Low}$, Time measured from V_{IN} 0V \rightarrow 5V 1 μs rise-time, to output turning ON		16		ms
I_{DD}	Operating current	$\overline{\text{CE}} = \text{Low}$, No load on OUT pin, $V_{\text{IN}} = 5\text{V}$, $R_{\text{(ILIM)}} = 25\text{k}\Omega$		580		μA
I_{STDBY}	Standby current	$\overline{\text{CE}} = \text{High}$, $V_{\text{IN}} = 5\text{V}$		75	95	μA
INPUT TO OUTPUT CHARACTERISTICS						
V_{DO}	Drop-out voltage IN to OUT	$\overline{\text{CE}} = \text{Low}$, $V_{\text{IN}} = 5\text{V}$, $I_{\text{OUT}} = 1\text{A}$		250	280	mV
OUTPUT VOLTAGE REGULATION						
$V_{\text{O(REG)}}$	Output voltage	$\overline{\text{CE}} = \text{Low}$, $V_{\text{IN}} = 5.7\text{V}$, $I_{\text{OUT}} = \text{No Load}$	5	5.15	5.30	V
INPUT OVERVOLTAGE PROTECTION						
V_{OVP}	Input overvoltage protection threshold	$\overline{\text{CE}} = \text{Low}$, V_{IN} increasing from 5V to 11V	6.65	6.8	6.95	V
$t_{\text{PD}}(\text{OVP})$	Input OV propagation delay ⁽¹⁾	$\overline{\text{CE}} = \text{Low}$		200		ns
$V_{\text{hys}}(\text{OVP})$	Hysteresis on OVP	$\overline{\text{CE}} = \text{Low}$, V_{IN} decreasing from 11V to 5V	20	100	110	mV
$t_{\text{ON}}(\text{OVP})$	Recovery time from input overvoltage condition	$\overline{\text{CE}} = \text{Low}$, Time measured from V_{IN} 7.5V \rightarrow 5V, 1 μs fall-time		16		ms
INPUT OVERCURRENT PROTECTION						
I_{OCP}	Input overcurrent protection threshold range		300		1500	mA
I_{OCP}	Input overcurrent protection threshold	$\overline{\text{CE}} = \text{Low}$, $R_{\text{(ILIM)}} = 15\text{k}\Omega$, $3\text{V} \leq V_{\text{IN}} < V_{\text{OVP}} - V_{\text{hys}}(\text{OVP})$	900	1000	1100	mA
$K_{\text{(ILIM)}}$	Adjustable current limit factor			15		A = k Ω
$t_{\text{BLANK}}(\text{OCP})$	Blanking time, input overcurrent detected			240		μs
$t_{\text{REC}}(\text{OCP})$	Recovery time from input overcurrent condition			128		ms
BATTERY OVERVOLTAGE PROTECTION						
BV_{OVP}	Battery overvoltage protection threshold	$\overline{\text{CE}} = \text{Low}$, $V_{\text{IN}} > 4.4\text{V}$	4.30	4.35	4.4	V
$V_{\text{hys}}(\text{BoVP})$	Hysteresis on BV_{OVP}	$\overline{\text{CE}} = \text{Low}$, $V_{\text{IN}} > 4.4\text{V}$	200	275	320	mV
$I_{\text{(VBAT)}}$	Input bias current on VBAT pin	$V_{\text{(VBAT)}} = 4.4\text{V}$, $T_{\text{J}} = 25^{\circ}\text{C}$			10	nA
$t_{\text{DGL}}(\text{BoVP})$	Deglitch time, battery overvoltage detected	$\overline{\text{CE}} = \text{Low}$, $V_{\text{IN}} > 4.4\text{V}$. Time measured from $V_{\text{(VBAT)}}$ rising from 4.1V to 4.4V to FAULT going low.		240		μs
THERMAL PROTECTION						
$T_{\text{J(OFF)}}$	Thermal shutdown temperature			140	150	$^{\circ}\text{C}$
$T_{\text{J(OFF-HYS)}}$	Thermal shutdown hysteresis			20		$^{\circ}\text{C}$
LOGIC LEVELS ON $\overline{\text{CE}}$						
V_{IL}	Low-level input voltage		0		0.4	V
V_{IH}	High-level input voltage		1.4			V
I_{IL}	Low-level input current	$V_{\text{(ICE)}} = 0\text{V}$			1	μA
I_{IH}	High-level input current	$V_{\text{(ICE)}} = 1.8\text{V}$			15	μA
LOGIC LEVELS ON FAULT						
V_{OL}	Output low voltage	$I_{\text{SINK}} = 5\text{mA}$			0.2	V
I_{Ikg}	Leakage current, FAULT pin HI-Z	$V_{\text{(FAULT)}} = 5\text{V}$			10	μA

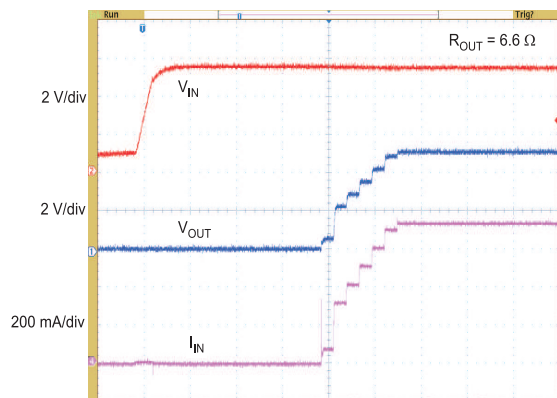
(1) Not tested in production. Specified by design.



TYPICAL PERFORMANCE CHARACTERISTICS

Test conditions (unless otherwise noted) for typical operating performance: $V_{IN} = 5\text{ V}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $R_{(LIM)} = 25\text{ k}\Omega$, $R_{BAT} = 100\text{ k}\Omega$, $T_A = 25^\circ\text{C}$, $V_{PU} = 3.3\text{ V}$

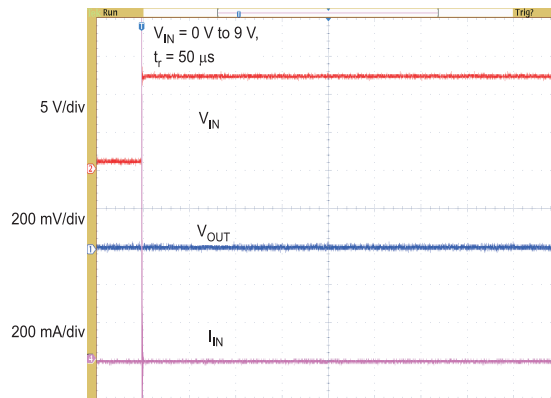
NORMAL POWER-ON SHOWING SOFT-START



t - Time - 2 ms/div

Figure 2.

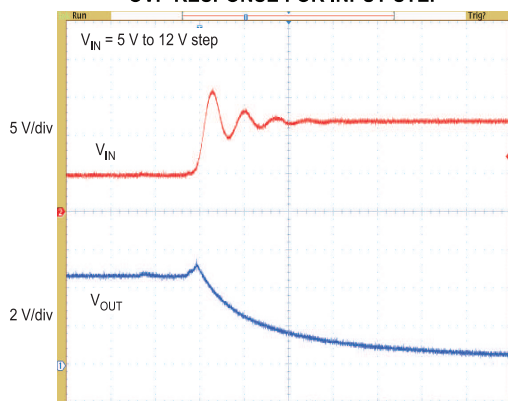
OVP AT POWER-ON



t - Time - 2 ms/div

Figure 3.

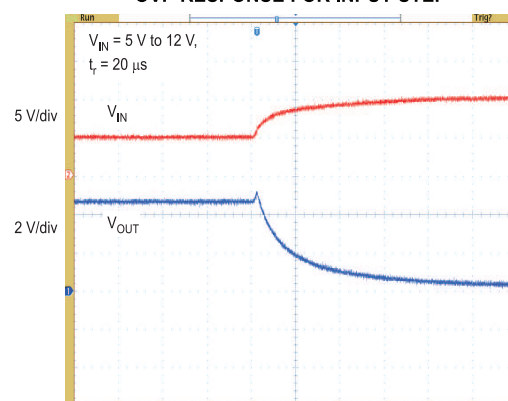
OVP RESPONSE FOR INPUT STEP



t - Time - 10 μs/div

Figure 4.

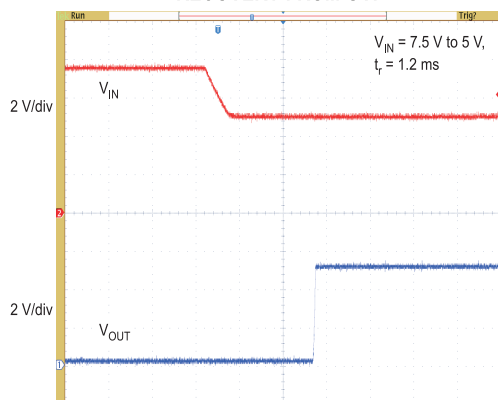
OVP RESPONSE FOR INPUT STEP



t - Time - 20 μs/div

Figure 5.

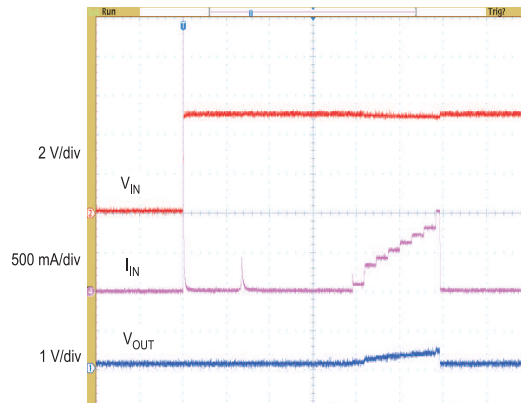
RECOVERY FROM OVP



t - Time - 4 ms/div

Figure 6.

OCP, ZOOM-IN ON THE FIRST CYCLE OF FIGURE 7



t - Time - 2 ms/div

Figure 7.



TYPICAL OPERATING PERFORMANCE (continued)

R_{OUT} SWITCHES FROM 6.6 Ω TO 3.3 Ω , SHOWS CURRENT LIMITING AND SOFT-STOP

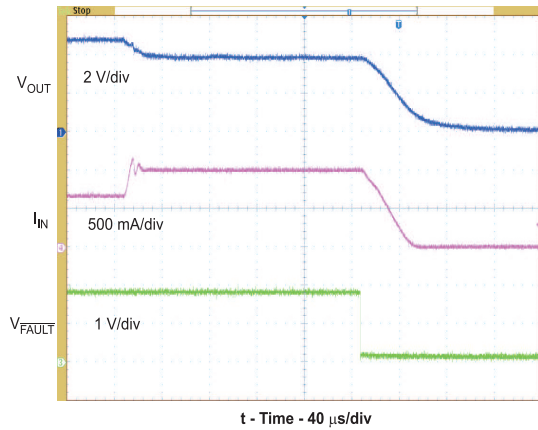


Figure 8.

BAT-OVP, $V_{(VBAT)}$ STEPS FROM 4 V TO 4.5 V, SHOWS $t_{DGL(BAT-OVP)}$ AND SOFT STOP

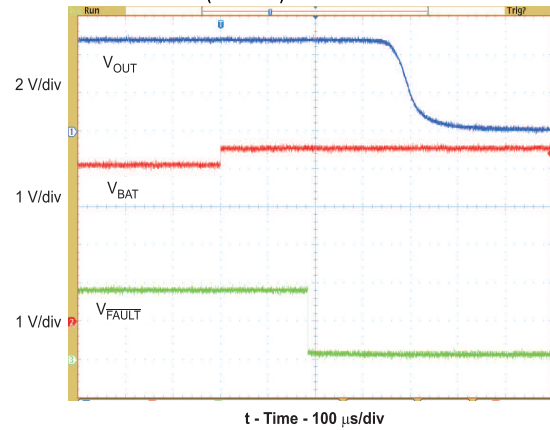


Figure 9 .

UNDERVOLTAGE LOCKOUT
vs
FREE-AIR TEMPERATURE

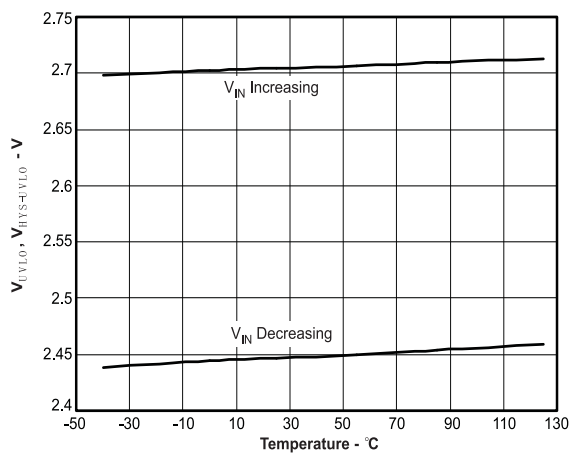


Figure 10.

DROPOUT VOLTAGE (IN to OUT)
vs
FREE-AIR TEMPERATURE

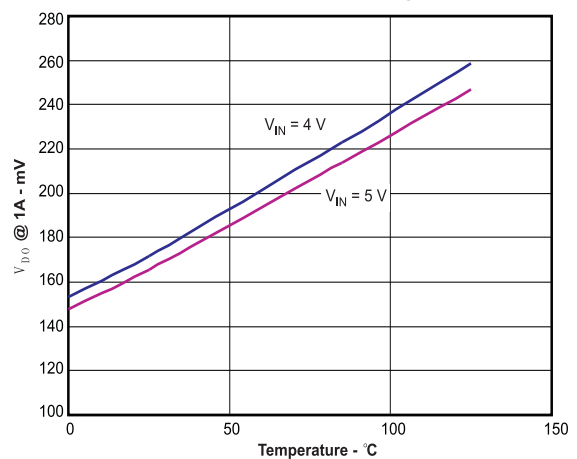


Figure 11.

OVERVOLTAGE THRESHOLD PROTECTION
vs
FREE-AIR TEMPERATURE

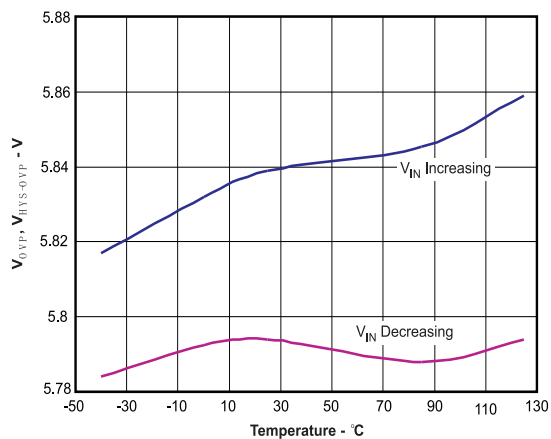


Figure 12.

INPUT OVERCURRENT PROTECTION
vs
ILIM RESISTANCE

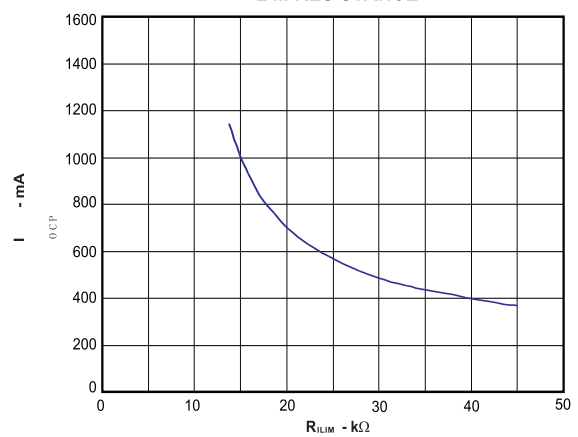


Figure 13.



TYPICAL OPERATING PERFORMANCE (continued)

INPUT OVERCURRENT PROTECTION
vs
FREE-AIR TEMPERATURE

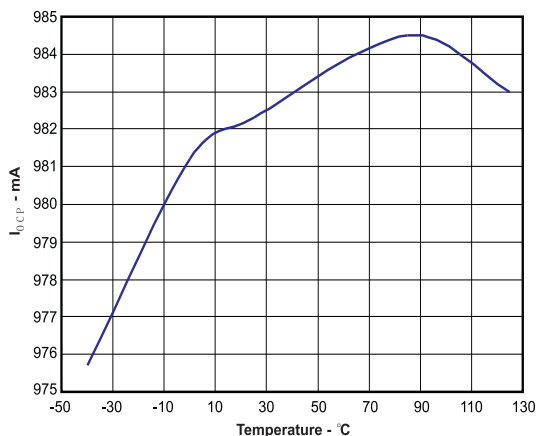


Figure 14.

BATTERY OVERVOLTAGE PROTECTION
vs
FREE-AIR TEMPERATURE

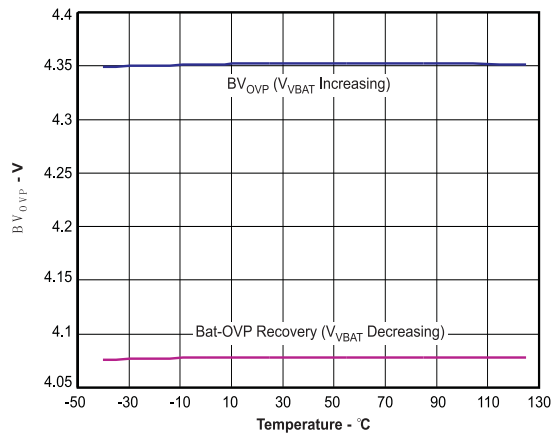


Figure 15.

LEAKAGE CURRENT (VBAT Pin)
vs
FREE-AIR TEMPERATURE

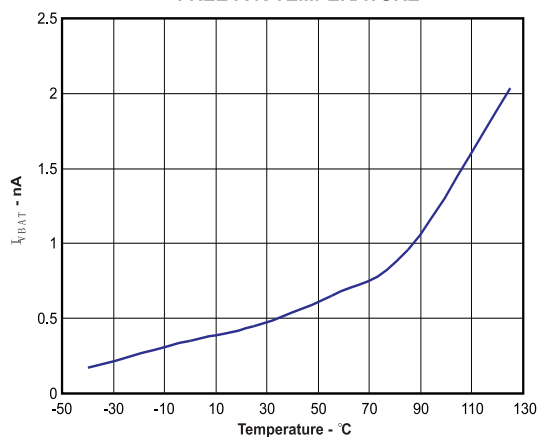


Figure 16.

SUPPLY CURRENT
vs
INPUT VOLTAGE

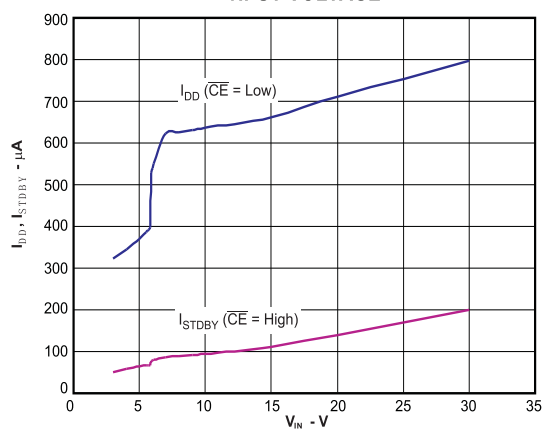
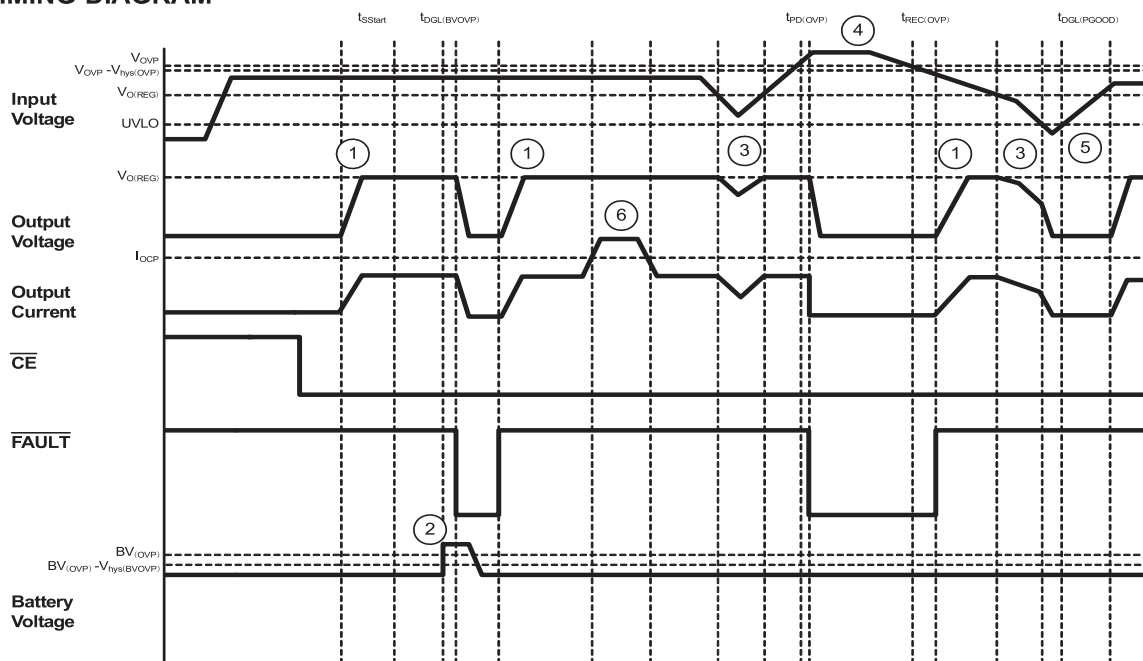


Figure 17.



TIMING DIAGRAM



1. Normal start-up condition
2. Battery over-voltage event
3. $V_{UVLO} < V_{IN} < V_{O(REG)}$, V_{OUT} tracks V_{IN}
4. Input over-voltage event
5. Input below $UVLO$
6. High-current event during normal operation

DETAILED FUNCTIONAL DESCRIPTION

CS5801T is a integrated circuits designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage, the input current and the battery voltage. For an input overvoltage condition, the IC immediately removes power from the charging circuit by turning off an internal switch. For an overcurrent condition, it limits the system current at the threshold value, and if the overcurrent persists, switches the pass element OFF after a blanking period. If the battery voltage rises to an unsafe level, the IC disconnects power from the charging circuit until the battery voltage returns to an acceptable value. Additionally, the IC also monitors its own die temperature and switches off if it exceeds 140°C. The input overcurrent threshold is user-programmable. The IC can be controlled by a processor, and also provides status information about fault conditions to the host.

POWER DOWN

The device remains in power down mode when the input voltage at the IN pin is below the undervoltage threshold $UVLO$. The FET Q1 connected between IN and OUT pins is off, and the status output, FAULT, is set to Hi-Z.

POWER-ON RESET

The device resets when the input voltage at the IN pin exceeds the $UVLO$ threshold. All internal counters and other circuit blocks are reset. The IC then waits for duration $t_{DGL(PGOOD)}$ for the input voltage to stabilize. If, after $t_{DGL(PGOOD)}$, the input voltage and battery voltage are safe, FET Q1 is turned ON. The IC has a soft-start feature to control the inrush current. The soft-start minimizes the ringing at the input (the ringing occurs because the parasitic inductance of the adapter cable and the input bypass capacitor form a resonant circuit). Because of the deglitch time at power-on, if the input voltage rises rapidly to beyond the OVP threshold, the device will not switch on at all, instead it will go into protection mode and indicate a fault on the FAULT pin.

OPERATION

The device continuously monitors the input voltage, the input current, and the battery voltage as described in detail in the following sections.

Input Overvoltage Protection

While the input voltage is less than $V_{O(REG)}$, the output voltage tracks the input voltage (less the drop due to the $R_{DS(on)}$ of Q1). When the input voltage is between $V_{O(REG)}$



and V_{OVP} , the device functions as a linear regulator and regulates the output voltage to 5.15V. If the input voltage rises above V_{OVP} , the internal FET Q1 is turned off, removing power to the output. The response is rapid, with the FET turning off in less than a microsecond. The \overline{FAULT} pin is driven low. When the input voltage returns below $V_{OVP} - V_{hys(OVP)}$ (but is still above UVLO), the FET Q1 is turned on again after a deglitch time of $t_{ON(OVP)}$ to ensure that the input supply has stabilized.

Input Overcurrent Protection

The overcurrent threshold is programmed by a resistor $R_{(ILIM)}$ connected from the ILIM pin to VSS. Figure 13 shows the OCP threshold as a function of $R_{(ILIM)}$, and may be approximated by the following equation: $I_{OCP} = 15 \div R_{(ILIM)}$ (current in A, resistance in k Ω)

If the load current tries to exceed the I_{OCP} threshold, the device limits the current for a blanking duration of $t_{BLANK(OCP)}$. If the load current returns to less than I_{OCP} before $t_{BLANK(OCP)}$ times out, the device continues to operate. However, if the overcurrent situation persists for $t_{BLANK(OCP)}$, the FET Q1 is turned off for a duration of $t_{REC(OCP)}$, and the \overline{FAULT} pin is driven low. The FET is then turned on again after $t_{REC(OCP)}$ and the current is monitored all over again.

To prevent the input voltage from spiking up due to the inductance of the input cable, Q1 is turned off slowly, resulting in a "soft-stop".

Battery Overvoltage Protection

The battery overvoltage threshold BV_{OVP} is internally set to 4.35V. If the battery voltage exceeds the BV_{OVP} threshold, the FET Q1 is turned off, and the \overline{FAULT} pin is driven low. The FET is turned back on once the battery voltage drops to $BV_{OVP} - V_{hys(Bovp)}$. For a battery overvoltage fault, Q1 is gradually switched OFF. The CS5801T have anti - access protection, if the battery error connected, the FET Q1 is turned off and the \overline{FAULT} pin is driven low.

Thermal Protection

If the junction temperature of the device exceeds $T_{J(OFF)}$, the FET Q1 is turned off, and the \overline{FAULT} pin is driven low. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} - T_{J(OFF-HYS)}$.

Enable Function

The IC has an enable pin which can be used to enable or disable the device. When the \overline{CE} pin is driven high, the internal FET is turned off. When the \overline{CE} pin is low, the FET is turned on if other conditions are safe. The \overline{CE} pin has an internal pulldown resistor and can be left floating. Note that the \overline{FAULT} pin functionality is also disabled when the \overline{CE} pin is high.

Fault Indication

The \overline{FAULT} pin is an active-low open-drain output. It is in a high-impedance state when operating conditions are safe, or when the device is disabled by setting \overline{CE} high. With \overline{CE} low, the \overline{FAULT} pin goes low whenever any of these events occurs:

- Input overvoltage
- Input overcurrent

- IC Overtemperature
- battery anti - access protection

APPLICATION INFORMATION (WITH REFERENCE TO FIGURE a)

Selection of R_{BAT}

It is strongly recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the IC, the voltage at the IN pin may appear on the VBAT pin. This voltage can be as high as 30V, and applying 30V to the battery in case of the failure of the CS5801T can be hazardous. Connecting the VBAT pin through R_{BAT} prevents a large current from flowing into the battery in case of a failure of the IC. In the interests of safety, R_{BAT} should have a high value. The problem with a large R_{BAT} is that the voltage drop across this resistor, due to the VBAT bias current $I_{(VBAT)}$, causes an error in the BV_{OVP} threshold. This error is over and above the tolerance on the nominal 4.35V BV_{OVP} threshold.

Choosing R_{BAT} in the range 100k Ω to 470k Ω is a good compromise. In the event of an IC failure, with R_{BAT} equal to 100k Ω , the maximum current flowing into the battery would be $(30V - 3V) \div 100k\Omega = 246\mu A$, which is low enough to be absorbed by the bias currents of the system components. R_{BAT} equal to 100k Ω results in a worst-case voltage drop of $R_{BAT} \times I_{(VBAT)} = 1mV$. This is negligible compared to the internal tolerance of 50mV on BV_{OVP} threshold.

If the Bat-OVP function is not required, the VBAT pin should be connected to VSS.

Selection of R_{CE} , R_{FAULT} , and R_{PU}

The \overline{CE} pin can be used to enable and disable the IC. If host control is not required, the \overline{CE} pin can be tied to ground or left un-connected, permanently enabling the device.

In applications where external control is required, the \overline{CE} pin can be controlled by a host processor. As in the case of the VBAT pin (see above), the \overline{CE} pin should be connected to the host GPIO pin through as large a resistor as possible. The limitation on the resistor value is that the minimum V_{OH} of the host GPIO pin less the drop across the resistor should be greater than V_{IH} of the CS5801T \overline{CE} pin. The drop across the resistor is given by $R_{CE} \times I_{IH}$.

The \overline{FAULT} pin is an open-drain output that goes low during OV, OC, battery-OV, and OT events. If the application does not require monitoring of the \overline{FAULT} pin, it can be left unconnected. But if the \overline{FAULT} pin has to be monitored, it should be pulled high externally through R_{PU} , and connected to the host through R_{FAULT} . R_{FAULT} prevents damage to the host controller if the CS5801T fails (see above). The resistors should be of high value, in practice values between 22k Ω and 100k Ω should be sufficient.

Selection of Input and Output Bypass Capacitors

The input capacitor C_{IN} in [Figure a](#) is for decoupling, and serves an important purpose. Whenever there is a step change downwards in the system load current, the inductance of the input cable causes the input voltage to spike up. C_{IN} prevents the input voltage from overshooting to dangerous levels. It is recommended that a ceramic capacitor of at least $1\mu F$ be used at the input of the device. It should be located in close proximity to the IN pin. C_{OUT} in [Figure a](#) is also important: If a fast ($< 1\mu s$ rise time) overvoltage transient occurs at the input, the current that charges C_{OUT} causes the device's current-limiting loop to start, reducing the gate-drive to FET Q1. This results in improved performance for input overvoltage protection. C_{OUT} should also be a ceramic capacitor of at least $1\mu F$, located close to the OUT pin. C_{OUT} also serves as the input decoupling capacitor for the charging circuit downstream of the protection IC.

Powering Accessories

In some applications, the equipment that the protection IC resides in may be required to provide power to an accessory (e.g. a cellphone may power a headset or an external memory card) through the same connector pins that are used by the adapter for charging. [Figure 18](#) and [Figure 19](#) illustrate typical charging and accessory-powering scenarios:

In the second case, when power is being delivered to an accessory, the CS5801T device is required to support current flow from the OUT pin to the IN pin.

If $V_{OUT} > UVLO + 0.7V$, FET Q1 is turned on, and the reverse current does not flow through the diode but through Q1. Q1 remains ON as long as $V_{OUT} > UVLO - V_{hys}(UVLO) + R_{DS(on)} \times I_{(ACCESSORY)}$. Within this voltage range, the reverse current capability is the same as the forward capability, 1.5A. It should be noted that there is no overcurrent protection in this direction.

PCB Layout Guidelines:

This device is a protection device, and is meant to protect down-stream circuitry from hazardous voltages. Potentially, high voltages may be applied to this IC. It has to be ensured that the edge-to-edge clearances of PCB traces satisfy the design rules for high voltages.

The device uses DFN2X2_8L packages with a PowerPAD™. For good thermal performance, the PowerPAD should be thermally coupled with the PCB ground plane. In most applications, this will require a copper pad directly under the IC. This copper pad should be connected to the ground plane with an array of thermal vias.

C_{IN} and C_{OUT} should be located close to the IC. Other components like $R_{(ILIM)}$ and R_{BAT} should also be located close to the IC.

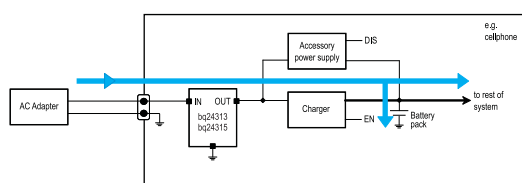


Figure 18 . Charging - The Red Arrows Show the Direction of Current Flow

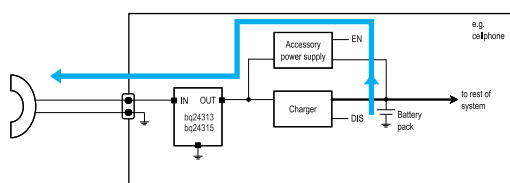
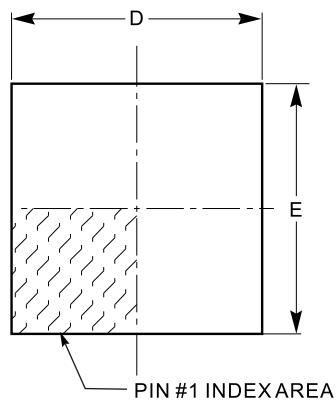


Figure 19 . Powering an Accessory - The Red Arrows Show the Direction of Current Flow

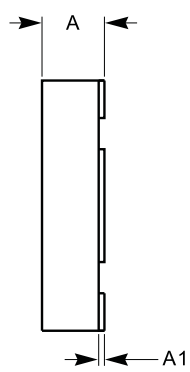


PACKAGE OUTLINE DIMENSIONS

CS5801T DFN 2X2_8L

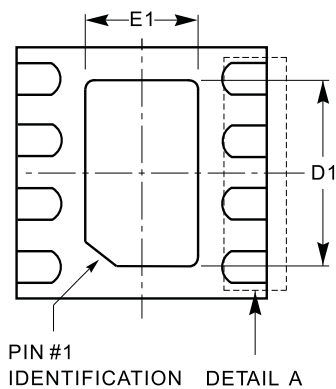


TOP VIEW

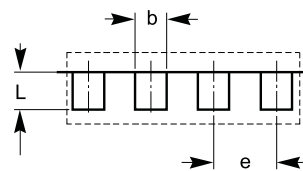


SIDE VIEW

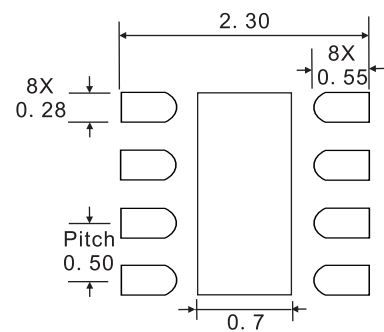
SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	2.00BSC		
D1	1.10	1.20	1.30
E	2.00BSC		
E1	0.50	0.60	0.70
e	0.50 BSC		
L	0.30	0.35	0.40



BOTTOM VIEW



DETAIL A



UNIT:mm