2×20W I²S输入免电感立体声D类音频功放

2×20W I²S Input, Inductor Free, Stereo Class D Amplifier

■ FEATURES

- Power supply:
  -PVDD: 4.5V – 16V; -DVDD/AVDD: 3.3V
- Audio Performance
  -BTL, 2×20W (PVDD=14.5V, R_L=4Ω, THD+N=1%)
  -PBTL, 24W (PVDD=15V, R_L=4Ω, THD+N=1%)
  -THD+N=0.04% (PVDD=12V, R_L=4Ω, Po=1W)
  -Noise: 100uV (Gain = 20dBV, A weighted)
- Low Quiescent Current
  -12mA at PVDD = 12V, no filter
- High efficiency in 1SPW mode (>90%)
- Inductor-free Operation (Ferrite Bead) and EMC compliant for most cases
- Flexible Audio I/O
  - I²S, LJ, RJ, TDM input
  - 8, 16, 32, 44.1, 48, 88.2, 96, 192kHz Sample Rates
- General Operational Features
  - Hardware or Software Control mode
  - 4 Programmable I²C Addresses
  - Spread Switching Frequency for Class D
- Robustness Features
  - Clock Error, DC, Over Current, Overvoltage, Undervoltage, and Overtemperature Protection
- Packages: Pb-free Packages, QFN28L-4×4

- 电源供电
  -PVDD: 4.5V – 16V; -DVDD/AVDD: 3.3V
- 音频性能
  -BTL, 2×20W (PVDD=14.5V,R_L=4Ω,THD+N=1%)
  -PBTL, 24W (PVDD=15V, R_L=4Ω, THD+N=1%)
  -THD+N=0.04% (PVDD=12V, R_L=4Ω, Po=1W)
  -噪声: 100uV (Gain = 20dBV, A加权)
- 低静态电流：12mA (PVDD = 12V, 无滤波器)
- 在1SPW模式下>90%的高效率
- 免电感滤波，在多数应用下仅磁珠即可过认证
- 灵活的音频输入：
  - I²S, LJ, RJ, TDM 输入
  - 8, 16, 32, 44.1, 48, 88.2, 96, 192kHz 采样频率
- 其他功能
  - 硬件模式或软件控制模式
  - 4个I²C器件地址可选
  - D类功放支持扩频功能
- 保护：时钟错误、直流、过流、过压、欠压、过温保护等
- QFN28L-4×4封装

■ APPLICATIONS

・Bluetooth/Wi-Fi Speakers	・Portable Speakers	・蓝牙/ Wi-Fi音箱	・便携式音箱
・Smart speakers	・Smart Home	・智能音箱	・智能家居
・Sound Bars	・TV/Monitor	・声霸	・TV/监视器

■ ORDERING INFORMATION

Part Number	Package Type	Marking	Operating Temperature Range	MOQ/Shipping Package
HT566SQER	QFN28L-4×4	HT566SQ UVWXYZ[1]	-25℃～85℃	Tape and Reel / 2500pcs

[1] UVWXYZ is production tracking code

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■ DESCRIPTION

The HT566 is a stereo Class D audio amplifier with multiple audio format port (I²S, LJ, RJ, TDM). It supports a variety of audio clock configurations.

The outputs of the HT566 can be configured to drive two speakers in stereo BTL mode or mono PBTL mode.

The HT566 also includes hardware and software control modes, integrated digital clipper, and a wide power supply operating range to enable use in a multitude of applications.

Advanced EMI Suppression with Spread Spectrum Control enables the use of inexpensive ferrite bead filters while meeting EMC requirements for system cost reduction.

An optimal mix of thermal performance and device cost is provided in the 120-mΩ $R_{DS(ON)}$ of the output MOSFETs. Additionally, a thermally enhanced 28-Pin QFN provides excellent operation in the elevated ambient temperatures found in modern consumer electronic devices.

HT566是一颗立体声D类音频功放，支持多种采样频率（8k-192kHz）、多种数字输入格式（I²S, LJ, RJ, TDM）。

HT566除了驱动BTL立体声双喇叭外，还能驱动PBTL单喇叭。

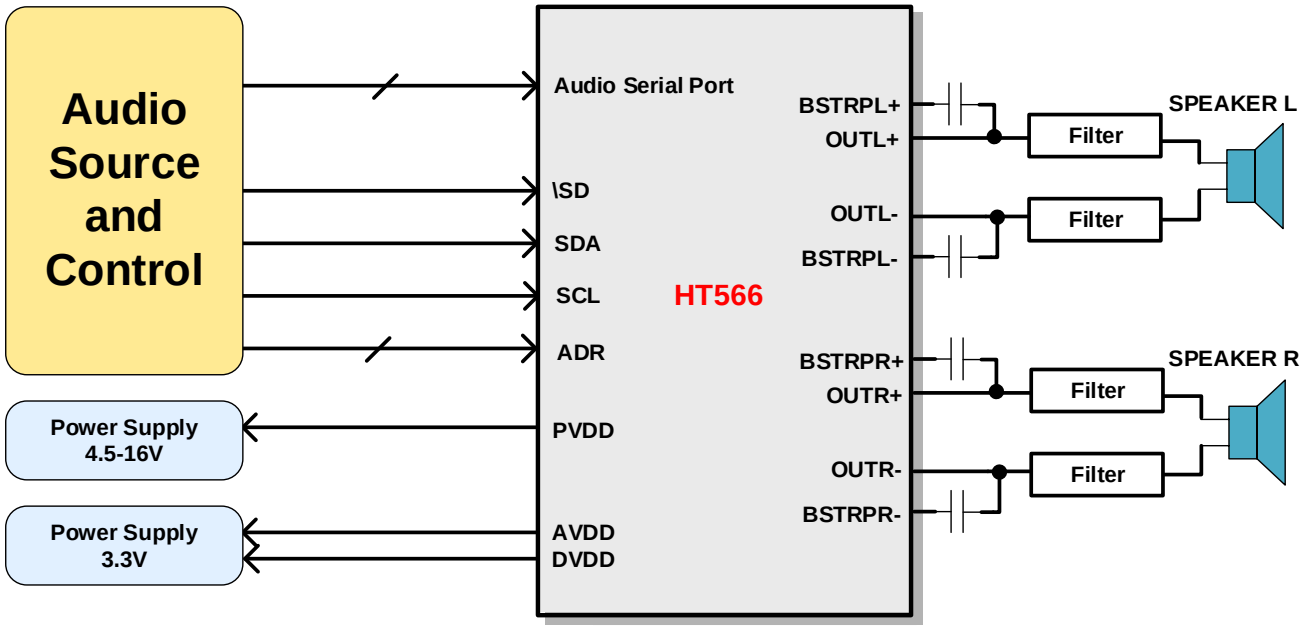
HT566包含了硬件工作模式和软件控制模式，具有数字限幅器，支持不同应用下较宽的工作电压范围。

具有扩频控制的EMI抑制功能，可在大多数应用情况下免除电感滤波器，仅使用低价的磁珠即可通过EMC认证。

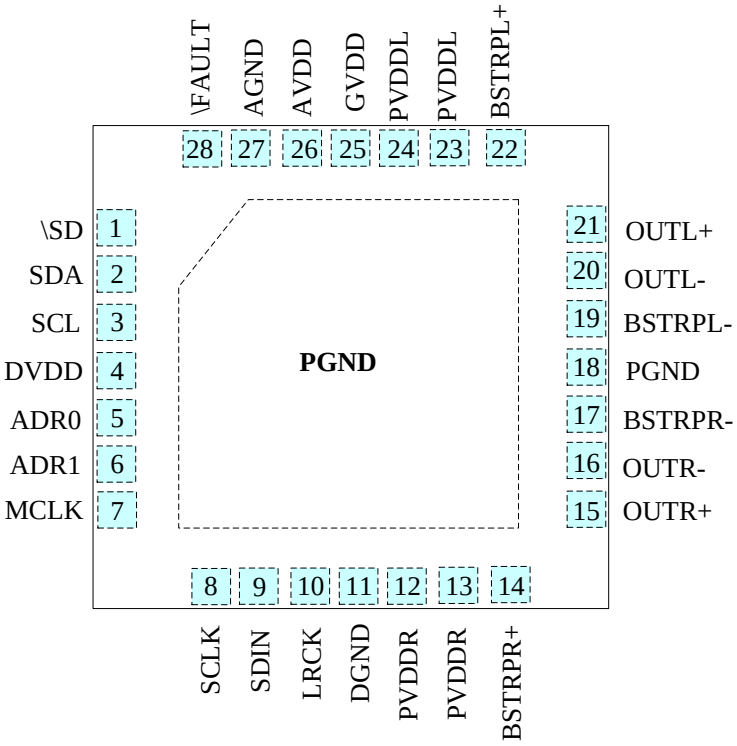
功放输出MOS的$R_{DS(ON)}$约为120mΩ，其在成本和散热表现二者间达到了最佳平衡。

该产品提供QFN28L-4×4封装，其具有不错的散热表现，在现代消费电子复杂的环境温度下提供出色的性能。

■ TYPICAL APPLICATION



■ TERMINAL CONFIGURATION



■ TERMINAL FUNCTION

Terminal No.	Name	I/O[1]	Description
1	\SD	I	Places the speaker amplifier in shutdown mode while pulled low level. 接地时功放关闭
2	SDA	I	I²C data input pin. I²C数据
3	SCL	I	I²C clock input terminal. I²C时钟
4	DVDD	P	Power supply for the internal digital circuitry. 数字电源端
5	ADR0	I	Determine the I²C Address of the device. I²C器件地址选择
6	ADR1	I	Determine the I²C Address of the device. I²C器件地址选择
7	MCLK	I	Master Clock used for internal clock tree, sub-circuit/state machine, and Serial Audio Port clocking. 主时钟
8	SCLK	I	Bit clock for the digital signal that is active on the serial data port's input data line. 串行时钟
9	SDIN	I	Data line to the serial data port. 串行数据
10	LRCK	I	Word select clock for the digital signal that is active on the serial port's input data line. 帧时钟，字段（声道）选择
11	DGND	G	Ground for digital circuitry (NOTE: This pin should be connected to the system ground). 数字地
12	PVDDR	P	Power Supply for internal power circuitry of Channel R. 右声道功率电源
13	PVDDR	P	
14	BSBRPR+	BST	Connection point for the OUTR+ bootstrap capacitor, which is used to create

1 : I: Input; O: Output; G: Ground; P: Power; BST: BOOT Strap; OD: Open drain

			a power supply for the high-side gate drive for OUTR+. OUTR+自举电容位
15	OUTR+	O	Positive pin for differential speaker amplifier output R. 右声道输出正端
16	OUTR-	O	Negative pin for differential speaker amplifier output R. 右声道输出负端
17	BSBRPR-	BST	Connection point for the OUTR- bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTR-. OUTR-自举电容位
18	PGND	G	Ground for power device circuitry (NOTE: This terminal should be connected to the system ground). 功率地
19	BSTRPL-	BST	Connection point for the OUTL- bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTL-. OUTL-自举电容位
20	OUTL-	O	Negative pin for differential speaker amplifier output L. 左声道输出负端
21	OUTL+	O	Positive pin for differential speaker amplifier output L. 左声道输出正端
22	BSBRPL+	BST	Connection point for the OUTL+ bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTL. OUTL+自举电容位
23	PVDDL	P	Power Supply for internal power circuitry of Channel L. 左声道功率电源
24	PVDDL	P	
25	GVDD	O	Voltage regulator derived from PVDD supply (NOTE: This pin is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry). 内部整流输出，接1uF电容到地
26	AVDD	P	Power supply for internal analog circuitry. 模拟电源端
27	AGND	G	Ground for analog circuitry (NOTE: This pin should be connected to the system ground). 模拟地
28	\FAULT	OD	Speaker amplifier fault terminal, which is pulled LOW when an internal fault occurs, open-drain output. 错误状态位，芯片发生某些错误时，该引脚拉低
EP	PGND	G	Provides both electrical and thermal connection from the device to the board. A matching ground pad must be provided on the PCB and the device connected to it via solder. For proper electrical operation, this ground pad must be connected to the system ground. 既是地，又是散热PAD

■ SPECIFICATIONS[1]

● Absolute Maximum Ratings [2]

PARAMETER	Symbol	MIN	TYP	MAX	UNIT
Power supply voltage for AVDD	AVDD	-0.3		4	V
Power supply voltage for PVDD	PVDD	-0.3		18	V
Power supply voltage for DVDD	DVDD	-0.3		4	V
DVDD Referenced Digital Input Voltages	V_I	-0.3		DVDD+0.3	V
Moisture Sensitivity Level (MSL)			MSL3		
Ambient Operating Temperature	T_A	-25		85	℃
Junction Temperature	T_J	-40		125	℃
Storage Temperature	T_{STG}	-40		125	℃

● Recommended Operating Conditions

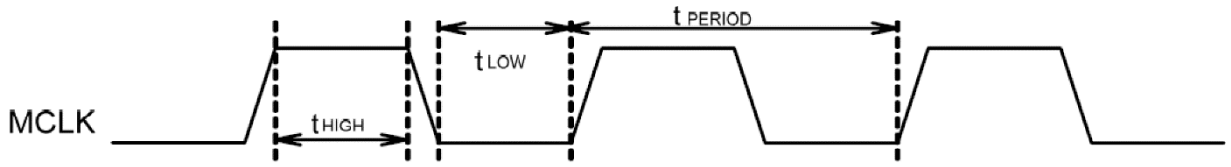
PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Power supply voltage for AVDD	AVDD		3	3.3	3.6	V
Power supply voltage for PVDD	PVDD		4.5		16	V
Power supply voltage for DVDD	DVDD		3	3.3	3.6	V
Ambient Operating Temperature	T_a		-25	25	85	℃
DVDD Referenced Digital Input Voltages	V_I		0		DVDD	V
Minimum Speaker Load in BTL Mode	R_L		4			Ω
Minimum Speaker Load in PBTL Mode	R_L		2			Ω

● I/O pins

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Input Logic High threshold for DVDD referenced digital inputs	V_{IH1}	All Digital I/O pins including \FAULT, \SD, SDA, SCL, ADR0, ADR1, MCLK, SCLK, SDIN, LRCK	70			%DVDD
Input Logic LOW threshold for DVDD Referenced Digital Inputs	V_{IL1}				30	%DVDD
Input Logic HIGH Current Level	I_{IH1}				15	uA
Input Logic LOW Current Level	I_{IL1}				-15	uA
Output Logic LOW Voltage Level	V_{OH}		90			%DVDD
Output Logic LOW Voltage Level	V_{OL}				10	%DVDD

● Master Clock

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Allowable MCLK Duty Cycle	D_{MCLK}		45	50	55	%
Supported MCLK Frequencies	f_{MCLK}	Values include: 128, 192, 256, 384, 512.	128		512	f_s
Pulse duration of MCLK high	t_{HIGH}		10.1			ns
Pulse duration of MCLK low	t_{LOW}		10.1			ns
Period of MCLK	t_{PERIOD}		20.2			ns

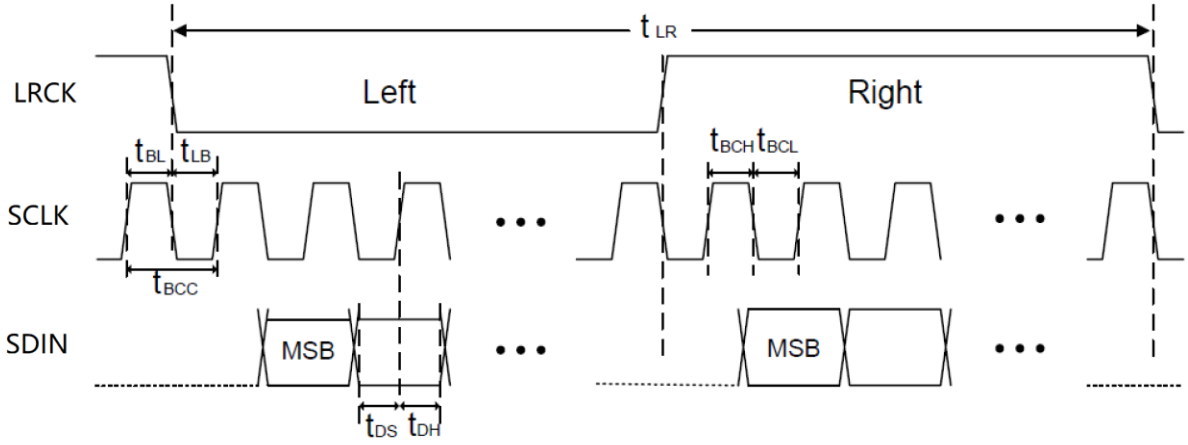


[1] Depending on parts and PCB layout, characteristics may be changed.

[2] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

Serial Audio Port

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Allowable SCLK Duty Cycle	D_{SCLK}		45	50	55	%
Supported Input Sample Rates ($1/t_{LR}$)	f_s		8		192	kHz
Required LRCK to SCLK Rising Edge	t_{LB}		15			ns
Required SCLK Rising Edge to LRCK edge	t_{BL}		15			ns
Supported SCLK Frequencies ($1/t_{BCC}$) for I2S	F_{SCLK}	Values include: 32, 48, 64	32		64	f_s
Supported SCLK Frequencies ($1/t_{BCC}$) for TDM	F_{SCLK}	Values include: 128, 256, 512	128		512	f_s
SCLK Pulse Width High	t_{BCL}			$t_{BCC}/2$		
SCLK Pulse Width Low	t_{BCH}			$t_{BCC}/2$		
Required SDIN Hold Time after SCLK, Rising Edge	t_{DH}		15			ns
Required SDIN Setup Time before SCLK Rising Edge	t_{DS}		15			ns



Protection Circuitry

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
PVDD Overvoltage Error Threshold	OVE_{RTH}	PVDD Rising		18		V
PVDD Overvoltage Error Threshold	OVE_{FTH}	PVDD Falling		17		V
PVDD Undervoltage Error Threshold	UVE_{RTH}	PVDD Falling		4.2		V
PVDD Undervoltage Error Threshold	UVE_{FTH}	PVDD Rising		4.4		V
Overtemperature Error Threshold	OTE_{TH}			150		℃
Overtemperature Error Hysteresis	OTE_{HYS}			15		℃
Overcurrent Error Threshold for each BTL Output	OCE_{TH}			7.5		A
DC Error Threshold	DCE_{TH}			2.6		V
Speaker Amplifier Fault Time Out period	T_{fault}	DCE or OTE or OCP		1.4		s

● Speaker Amplifier in All Modes

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Speaker Amplifier Gain	AV_{00}			20		dBV
Speaker Amplifier DC Offset	$\|V_{OS}\|$	BTL		1.5		mV
Speaker Amplifier Switching Frequency	$f_{SPK\_AMP(1)}$			360		kHz
On Resistance of Output MOSFET (both high-side and low-side)	$R_{DS(ON)}$			120		mΩ
–3-dB Corner Frequency of High-Pass Filter	f_C	f_S = 44.1 kHz		3.7		Hz
		f_S = 48 kHz		4		Hz
		f_S = 88.2 kHz		7.4		Hz
		f_S = 96 kHz		8		Hz

● Speaker Amplifier in Stereo Bridge Tied Load (BTL) Mode

TA = 25°, PVDD = 12V, DVDD = AVDD = 3.3V, BTL mode, GAIN = 20dBV, BD mode, fs = 48kHz (unless otherwise noted)

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Idle Channel Noise	V_N	PVDD = 12 V, GAIN =20dBV, R_{SPK} = 8 Ω or 4 Ω, 20-20kHz, A-Weighted		100		μV
Signal to Noise Ratio (Referenced to THD+N=1%)	SNR	PVDD = 12 V, R_{SPK} = 8 Ω or 4Ω, 20-20kHz, A-Weighted		97		dB
Maximum Instantaneous Output Power Per. Ch.	Po	PVDD = 12 V, R_{SPK} = 4 Ω, THD+N = 1%		14		W
		PVDD = 12 V, R_{SPK} = 8 Ω, THD+N = 1%		8		W
		PVDD = 14.5V, R_{SPK} = 4 Ω, THD+N = 1%		20		W
		PVDD = 15 V, R_{SPK} = 8 Ω, THD+N = 1%		12.5		W
Total Harmonic Distortion and Noise	THD+N	PVDD = 12 V, R_{SPK} = 4 Ω, Po = 1 W		0.02		%
		PVDD = 12 V, R_{SPK} =8 Ω, Po = 1 W		0.02		%
Cross-talk (worst case between L->R and R->L coupling)	X-Talk	PVDD = 12 V, GAIN = 16dBV, R_{SPK} = 4 Ω, Po = 1W		-85		dB

● Speaker Amplifier in Mono Parallel Bridge Tied Load (PBTL) Mode

TA = 25°, PVDD = 12V, DVDD = AVDD = 3.3V, BTL mode, GAIN = 20dBV, BD mode, fs = 48kHz (unless otherwise noted)

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Idle Channel Noise	V_N	PVDD = 12 V, GAIN = 16dBV, R_{SPK} = 8 Ω or 4 Ω, 20-20kHz, A-Weighted		100		μV
Signal to Noise Ratio (Referenced to THD+N =1%)	SNR	PVDD = 12 V, R_{SPK} = 8 Ω or 4Ω, 20-20kHz, A-Weighted		97		dB
Maximum Instantaneous Output Power.	Po	PVDD = 12 V, R_{SPK} = 4 Ω, THD+N = 1%		16		W
		PVDD = 12 V, R_{SPK} = 2 Ω, THD+N = 1%		26		W
		PVDD = 15 V, R_{SPK} = 4 Ω, THD+N = 1%		24		W
		PVDD = 15 V, R_{SPK} = 3 Ω, THD+N = 1%		30		W
Total Harmonic Distortion and Noise	THD+N	PVDD = 12 V, R_{SPK} = 4 Ω, Po = 1 W		0.02		%
		PVDD = 12 V, R_{SPK} = 2 Ω, Po = 1 W		0.03		%

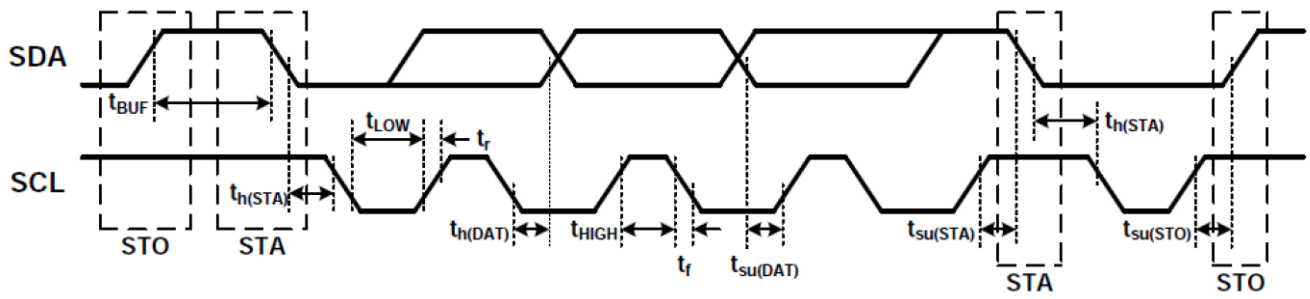
● Typical current consumption

TA = 25°, PVDD = 12V, DVDD = AVDD = 3.3V, No Load, BTL mode, GAIN = 20dBV, BD mode, fs = 48kHz, (unless otherwise noted)

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
$I_{DVDD+AVDD}$						
Quiescent current in DVDD+AVDD	$I_{DVDD+AVDD}$	fs=48kHz MCLK=128*fs		4.5		mA
		fs=48kHz MCLK=256*fs		5.3		mA
		fs=48kHz MCLK=512*fs		5.5		mA
		fs=32kHz MCLK=128*fs		6.7		mA
		fs=32kHz MCLK=256*fs		8.3		mA
		fs=32kHz MCLK=512*fs		8.8		mA
DVDD+AVDD current consumption in sleep mode	$I_{DVDD+AVDD\_SLEEP}$	SLEEP = H, fs=48kHz MCLK=256*fs		3.0		mA
		SLEEP = H, fs=32kHz MCLK=256*fs		3.5		mA
DVDD+AVDD current consumption in SD mode	$I_{DVDD+AVDD\_SD}$	\SD = L, No clock		120		uA
IPVDD						
Quiescent current in PVDD	IPVDD	PVDD=12V		12		mA
PVDD current consumption in Amplifier MUTEA Mode (MUTE_A)	I_{PVDD_MUTEA}	PVDD=12V		6		mA
PVDD current consumption in SD mode	I_{PVDD_SD}	PVDD=12V		12		uA

● I²C Control Port

PARAMETER	Symbol	Standard-Mode			Fast-Mode			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Allowable Load Capacitance for Each I²C Line	C_b			400			400	pF
Support SCL frequency	f_{SCL}			100			400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{h(STA)}$	4			0.6			us
Required Pulse Duration, SCL HIGH	t_{HIGH}	4			0.6			us
Required Pulse Duration, SCL LOW	t_{LOW}	4.7			1.3			us
Setup time for a repeated START condition	$t_{su(STA)}$	4.7			0.6			us
Data hold time	$t_{h(DAT)}$	0		3.45	0		0.9	us
Setup Time, SDA to SCL	$t_{su(DAT)}$	250			100			ns
Rise Time, SCL	T_{r_SCL}			1000			300	ns
Rise Time, SDA	T_{r_SDA}			$1/(4*f_{scl})$-0.25			$1/(4*f_{scl})$-0.25	us
Fall Time, SCL and SDA	T_f			300			300	ns
Setup Time, SCL to STOP condition	$t_{su(STO)}$	4			0.6			us
Bus Free time between STOP and START conditions	t_{BUF}	4.7			1.3			us



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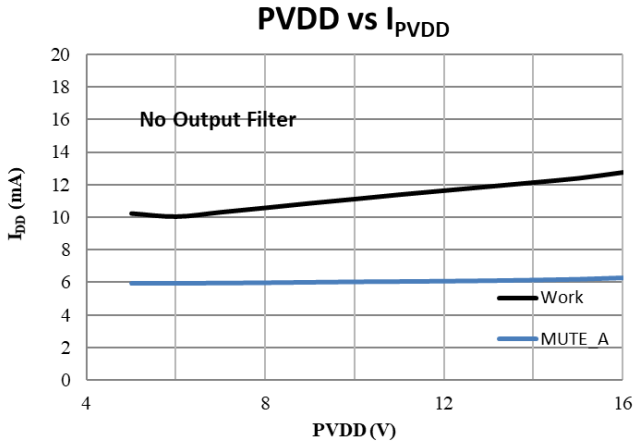
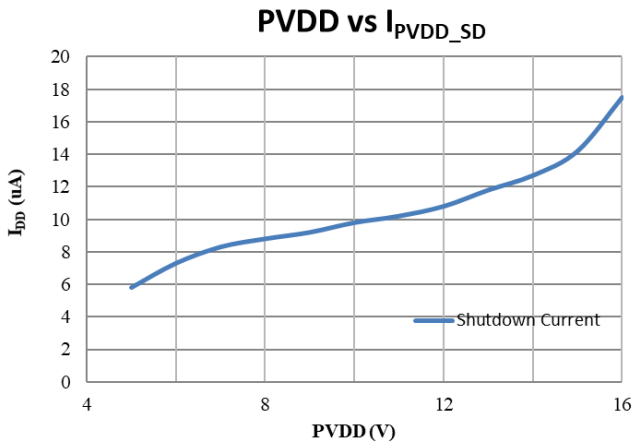
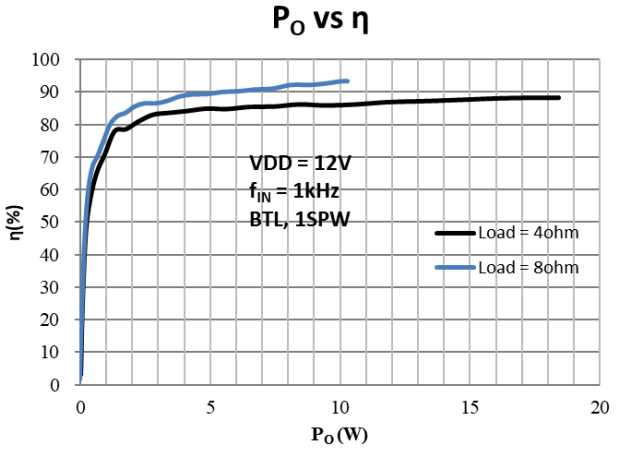
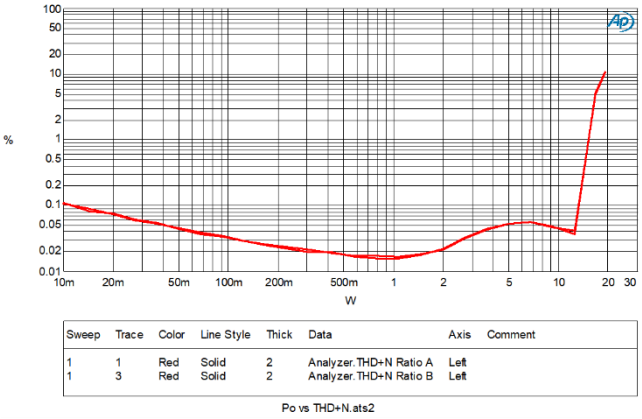
■ TYPICAL OPERATING CHARACTERISTICS

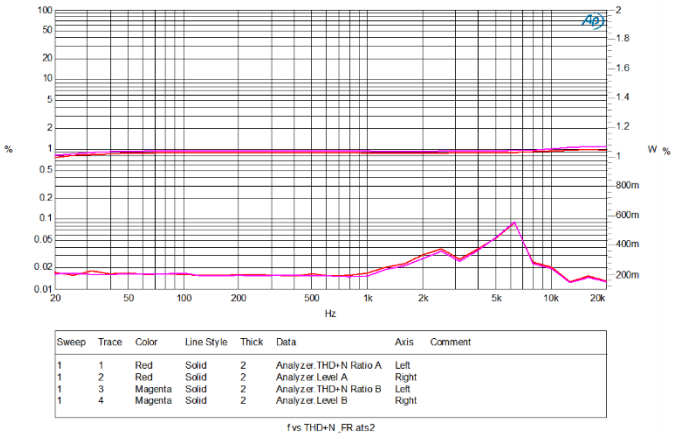


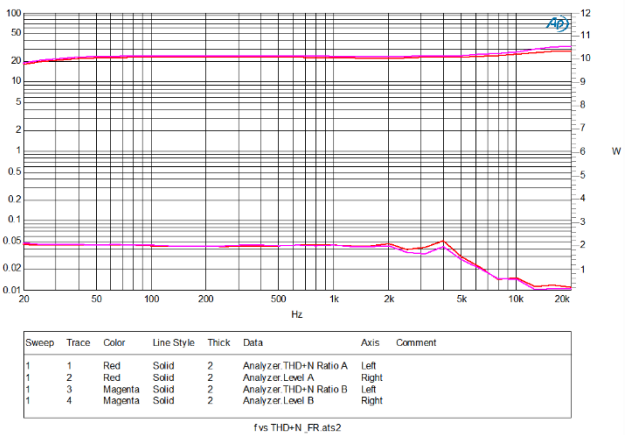


T_A = 25°C, PVDD =12V, DVDD = 3.3V, **BTL mode**, f_{IN} = 1 kHz, BD mode, Load = 4ohm, No LC filter, unless otherwise noted.



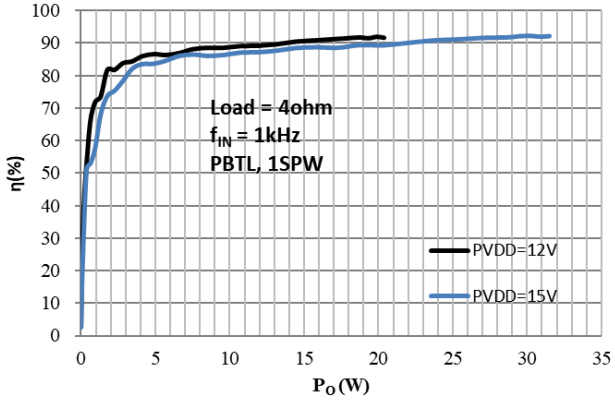


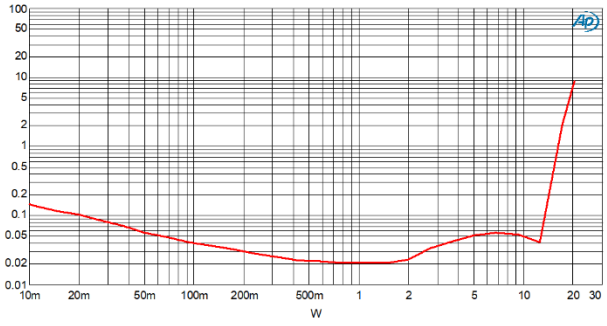




T_A = 25°C, PVDD =12V, **PBTL mode**, f_{IN} = 1 kHz, BD mode, Load = 4ohm, No LC filter, unless otherwise noted.

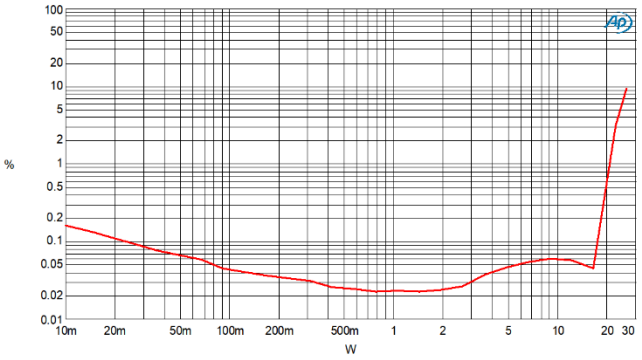
P_O vs η





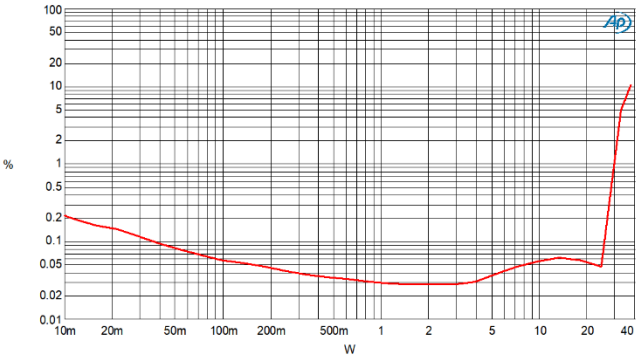
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Analyzer.THD+N Ratio A	Left	Load = 4ohm

Po vs THD+N.ats2



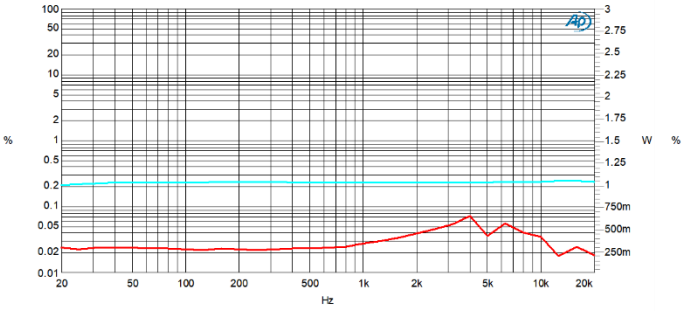
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Analyzer.THD+N Ratio A	Left	Load = 3ohm

Po vs THD+N.ats2



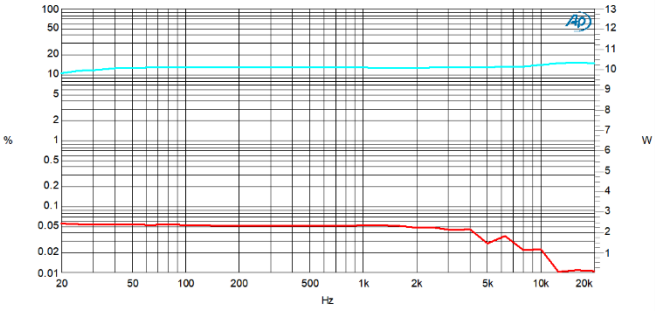
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Analyzer.THD+N Ratio A	Left	Load = 2ohm

Po vs THD+N.ats2



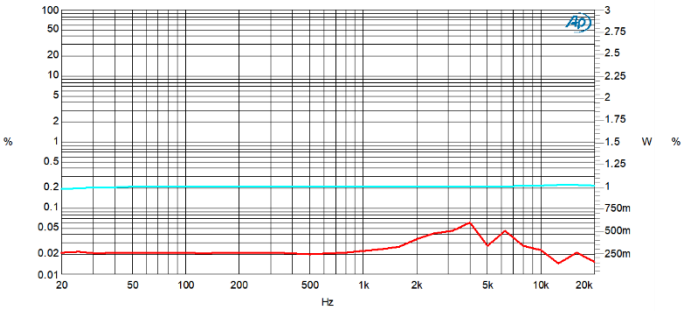
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Analyzer.THD+N Ratio A	Left	Load = 2ohm
1	2	Cyan	Solid	2	Analyzer.Level A	Right	Load = 2ohm

f vs THD+N _FR.ats2



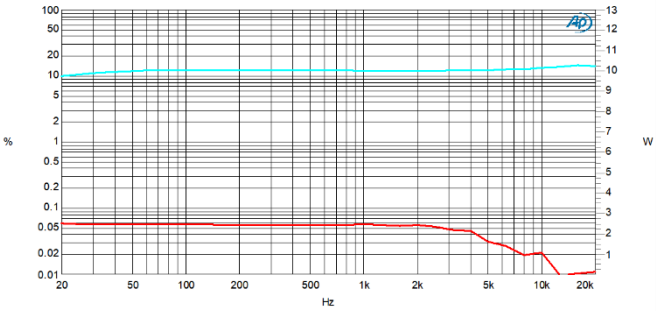
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Analyzer.THD+N Ratio A	Left	Load = 2ohm
1	2	Cyan	Solid	2	Analyzer.Level A	Right	Load = 2ohm

f vs THD+N _FR.ats2



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Analyzer.THD+N Ratio A	Left	Load = 3ohm
1	2	Cyan	Solid	2	Analyzer.Level A	Right	Load = 3ohm

f vs THD+N _FR.ats2



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Analyzer.THD+N Ratio A	Left	Load = 3ohm
1	2	Cyan	Solid	2	Analyzer.Level A	Right	Load = 3ohm

f vs THD+N _FR.ats2

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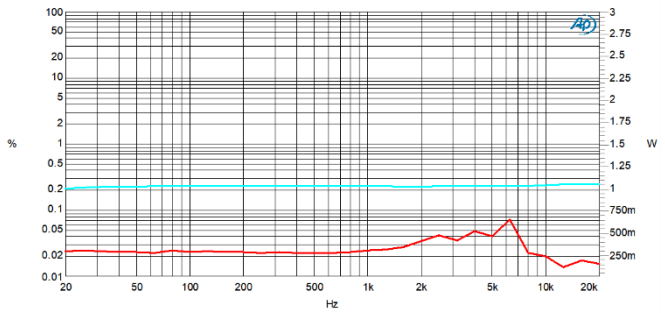
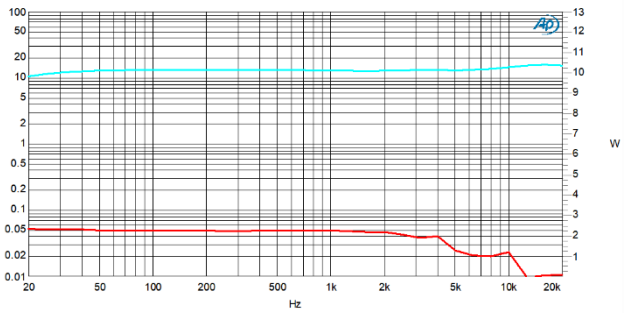


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Analyzer.THD+N Ratio A	Left	Load = 4ohm
1	2	Cyan	Solid	2	Analyzer.Level A	Right	Load = 4ohm

f vs THD+N_FR.ats2



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Analyzer.THD+N Ratio A	Left	Load = 4ohm
1	2	Cyan	Solid	2	Analyzer.Level A	Right	

f vs THD+N_FR.ats2

■ APPLICATION INFORMATION

The HT566 is a flexible and easy-to-use stereo class-D speaker amplifier with an digital input serial audio port. The HT566 supports a variety of audio clock between 8kHz to 192kHz sample rate. The outputs of the HT566 can be configured to drive two speakers in stereo Bridge Tied Load (BTL) mode or a single speaker in Parallel Bridge Tied Load (PBTL) mode.

HT566 是一颗简单易用且灵活的数字输入 D 类音频功放，其支持 8k~192kHz 的采样频率。HT566 的输出可配置成立体声双喇叭 BTL 输出，或单通道单喇叭 PBTL 输出。

1 Power Supplies

Only two power supplies are required for the HT566. They are a 3.3-V power supply, called DVDD and AVDD for the small signal digital and analog and a higher voltage power supply, called PVDD for the output stage of the speaker. To enable use in a variety of applications, PVDD can be operated over a large range of voltages, which is 4.5V – 16V, and it is recommended to put paralleled capacitor of 100nF//1uF//220uF between each channel of PVDD and system ground.

HT566 仅需要两种电源供电，即在 DVDD（数字电源）和 AVDD（模拟电源）端加 3.3V，在 PVDD（功率电源）端加 4.5-16V。，每个通道的 PVDD 端建议各加 100nF//1uF//220uF 的并联电容到地。

2 Speaker Amplifier Audio Signal Path

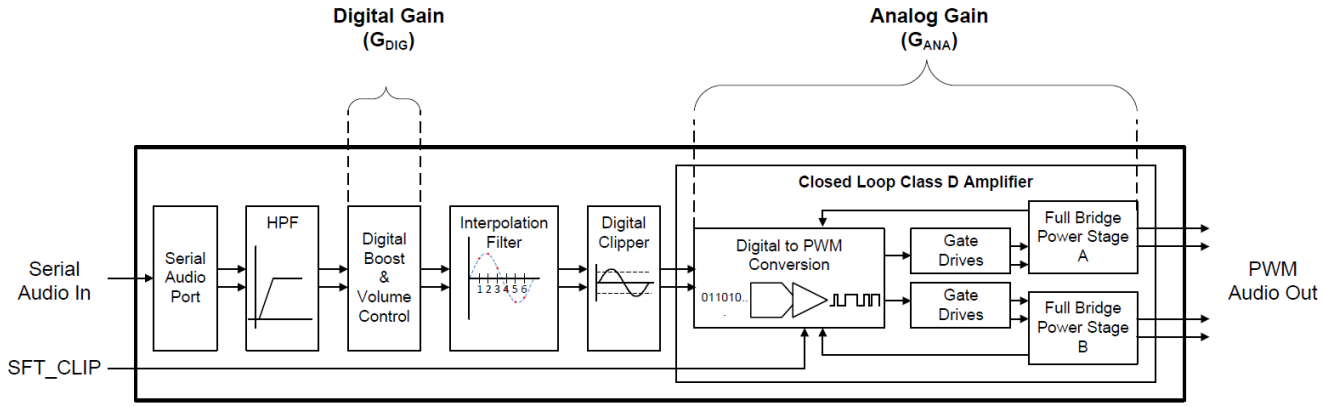


Figure 1 Speaker Amplifier Audio Signal Path

2.1 Serial Audio Port

The serial audio port receives audio in either I²S, Left Justified, Right Justified or TDM formats, up to 32-bit word length. Default setting is I²S and 32-bit word length. The supported clock rates and ratios are detailed below.

HT566 的数字音频串行输入接口支持 I²S、左对齐、右对齐、TDM 等数据格式，最高支持 32 bit 字长（SCLK = 32×2 fs）。默认设置为 I²S、32 bit 字长。支持的相关时钟速率和比例如下表。

Table1 Supported SCLK rates for TDM

Maximum Sample Rate fs (kHz)	SCLK Rate (xfs)
8-48kHz	128, 256, 512
96kHz	128, 256
192kHz	128

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Table2 Supported SCLK rates for IIS/LJ/RJ

Sample Rate fs (kHz)	MCLK rate (× fs)							
	128	192	256	384	512	768	1024	1152
	SCLK rate (× fs)							
8	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S	N/S
12	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S	N/S
16	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S
24	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S
32	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
38	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S
44.1	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S
48	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S
64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S	N/S
88.2	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S	N/S	N/S	N/S
96	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S	N/S	N/S	N/S
128	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	N/S	N/S	N/S	N/S
176.4	32, 48, 64	32, 48, 64	N/S	N/S	N/S	N/S	N/S	N/S
192	32, 48, 64	32, 48, 64	N/S	N/S	N/S	N/S	N/S	N/S

2.1.1 I²S

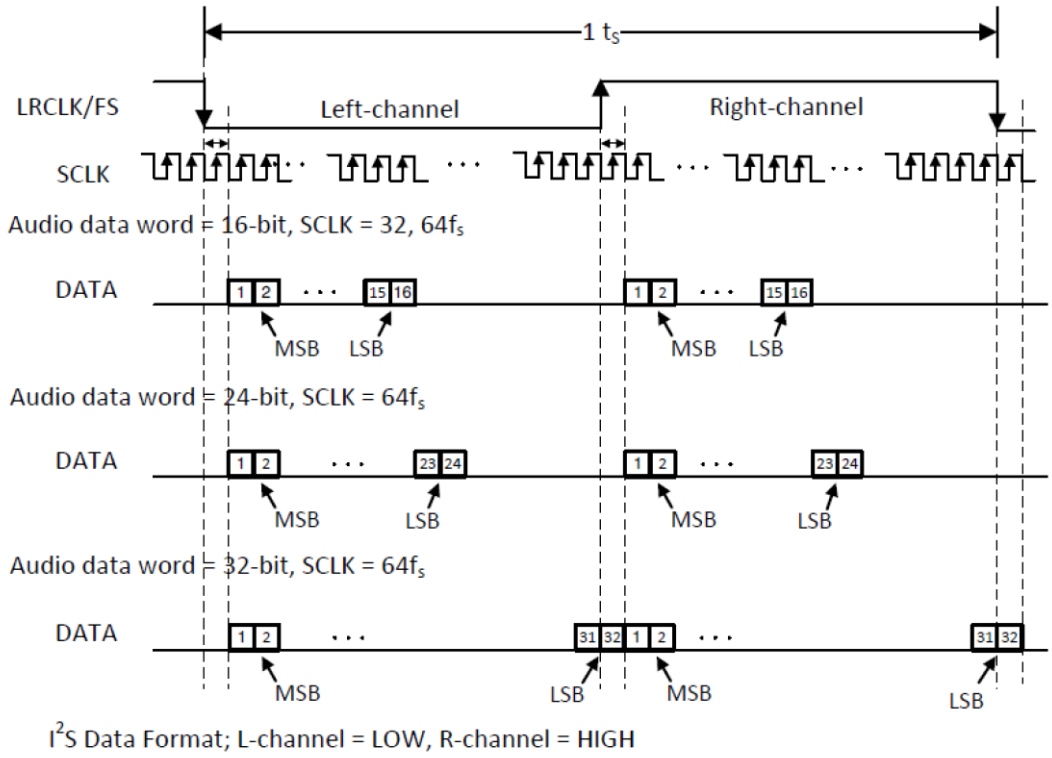

Figure 2 IIS Audio Data Format Timing

2.1.2 Left-Justified

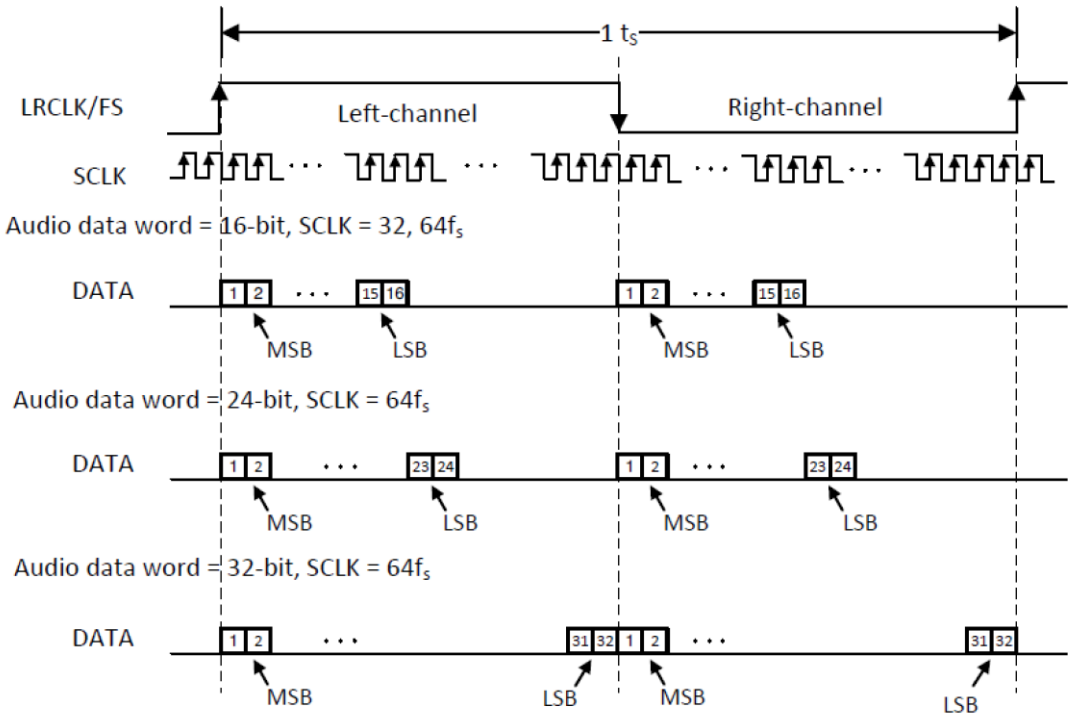

Figure 3 Left-Justified Audio Data Format Timing

2.1.3 Right-Justified

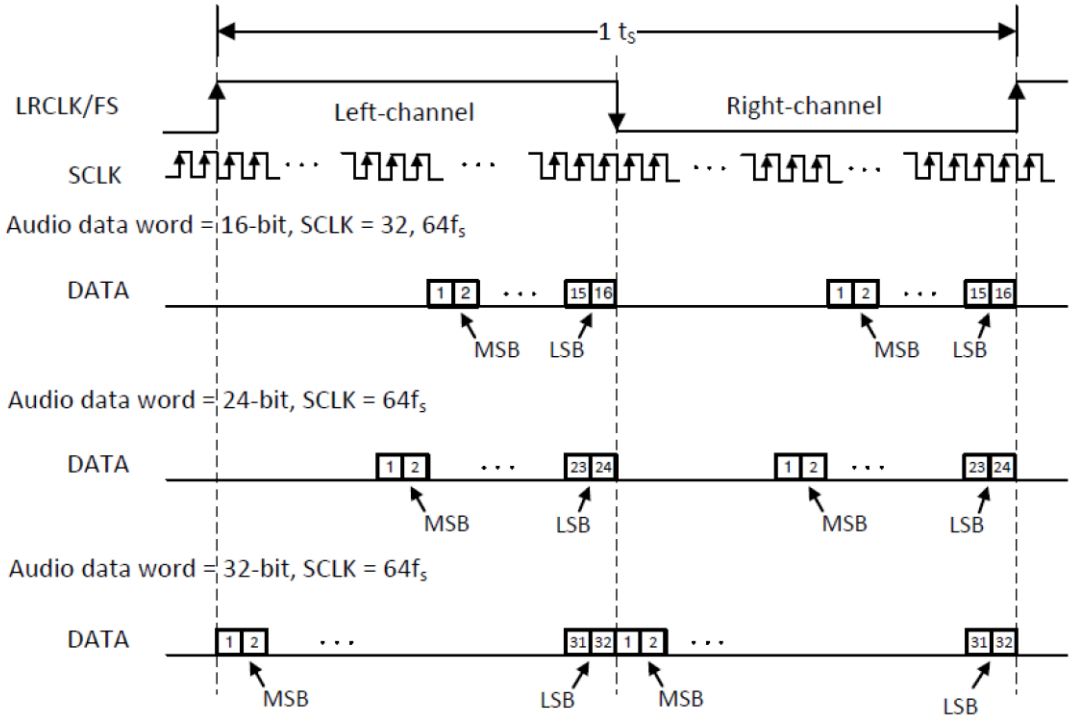

Figure 4 Right-Justified Audio Data Format Timing

2.1.4 TDM

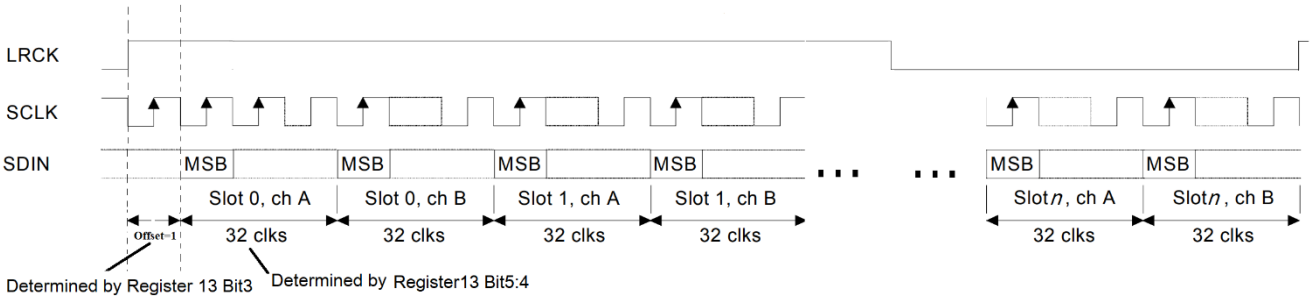

Figure 5 TDM Audio Data Format Timing

2.2 DC Blocking Filter

Excessive DC content in the audio signal can damage loudspeakers and even small amounts of DC offset in the signal path cause audible artifacts when muting and unmuting the speaker amplifier. For these reasons, the amplifier employs two separate DC blocking methods for the speaker amplifier. The first is a high-pass filter provided at the front of the data path to remove any DC from incoming audio data before it is presented to the audio path. The –3 dB corner frequencies for the filter are specified in the speaker amplifier electrical characteristics table. In Hardware Control mode, the DC blocking filter is active and cannot be disabled. In software Control mode, the filter can be bypassed by writing a 0 to bit 7 of register 0x14. The second method is a DC detection circuit that will shut down the power stage if DC is found to be present on the output due to some internal error of the device. This DC Error (DCE) protection is discussed in the **DC Detect Protection** below.

音频信号持续的直流成分，可能损坏喇叭，或者产生输出直流偏置进而在静音/解除静音时产生噪声。因此，HT566 具有两种隔直流的方式。

一种是在数据通道前端设置高通滤波器，以在数据输入端去除直流成分。该滤波器的截止频率已在上面参数表中列出。在硬件工作模式，该滤波器不能关闭；在软件控制模式，该滤波器可关闭（0x14 寄存器的 bit7）。

另一种是 DC 检测电路，当其检测到输出端有一定的直流成分的时候，HT566 将关闭芯片。这种 DCE 保护将在下面 **DC Detect Protection** 描述。

2.3 Digital Boost and Volume Control

Following the high-pass filter, a digital boost block is included to provide additional digital gain if required for a given application as well as to set an appropriate clipping point for a given GAIN configuration. The digital boost block defaults to +0dB and is changeable through bit [1:0] of register 14. In most use cases, the digital boost block will remain unchanged, as the volume control offers sufficient digital gain for most applications. The HT566's digital volume control operates from Mute to 24 dB, in steps of 0.5 dB. The equation below illustrates how to set the 8-bit volume control register at address 0x15/0x16:

DVC [Hex Value] = 0xCF + (DVC [dB] / 0.5 [dB])

Transitions between volume settings will occur at a rate of 0.5 dB every 8 LRCK cycles to ensure no audible artifacts occur during volume changes. This volume fade feature can be disabled via Bit 4 of Register 0x14.

在高通滤波隔直后是数字增加模块，该模块可为数字信号提供一个附加的数字增益，以适应不同的应用。其默认设置是+0dB，可通过 0x14 寄存器的 bit[1:0]修改。在大多数情况下，其设置后不用修改。

HT566 的数字音量控制可通过 0x15 和 0x16 寄存器设置 Mute~+24dB（每步 0.5dB）。下面是如何设置该寄存器的公式：

DVC [Hex Value] = 0xCF + (DVC [dB] / 0.5 [dB])

数字音量的变化速率为 0.5dB/8LRCK，以避免音量突变产生噪声。这种音量渐变的功能可通过 0x14 寄存器的 bit4 关闭。

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2.4 Digital Clipper

A digital clipper is integrated in the oversampled domain to provide a component-free method to set the clip point of the speaker amplifier. Through the "Digital Clipper Level x" (at register address 0x10, 0x11, 0x12) controls in the I²C control port, the point at which the oversampled digital path clips can be set directly, which in turns sets the 10% THD+N operating point of the amplifier. This is useful for applications in which a single system is designed for use in several end applications that have different power rating specifications. Its place in the oversampled domain ensures that the digital clipper is acoustically appealing and reduces or eliminates tones which would otherwise foldback into the audio band during clipping events. Figure 6 shows a block diagram of the digital clipper.

HT566 集成了数字限幅器，无需任何元器件、仅通过寄存器（0x10, 0x11, 0x12）配置即可设置功放输出的削顶幅度，即功放 10% THD+N 工作点。其在一种硬件设计适应多种不同功率等级的应用终端时特别有用。

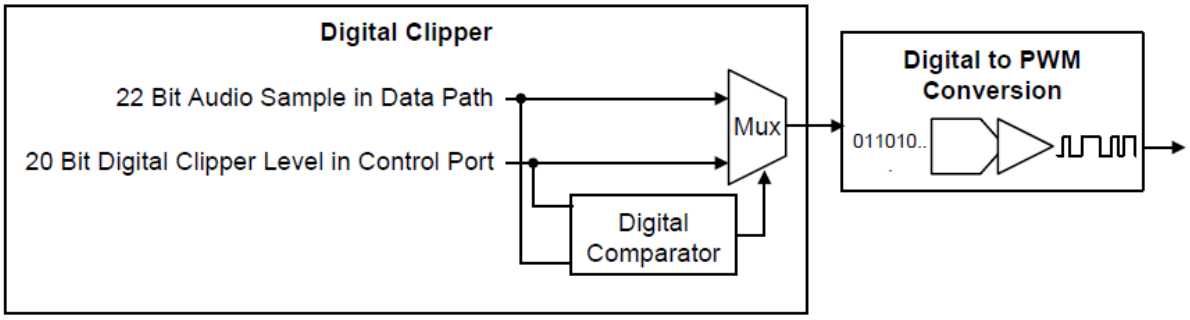

Figure 6 Digital Clipper Simplified Block Diagram

It is important to note that the actual signal developed across the speaker will be determined not only by the digital clipper, but also the analog gain of the amplifier. Depending on the analog gain settings and the PVDD level applied, clipping could occur as a result of the voltage swing that is determined by the gain being larger than the available PVDD supply rail.

需要了解的是，功放输出的最终幅度不止取决于该限幅器，还取决于当前设置的模拟增益和 PVDD 电压。

2.5 Closed-Loop Class-D Amplifier

Following the digital clipper, the interpolated audio data is next sent to the Closed-Loop Class-D amplifier, whose first stage is Digital to PWM Conversion (DPC) block. In this block, the stereo audio data is translated into two pairs of complimentary pulse width modulated (PWM) signals which are used to drive the outputs of the speaker amplifier. Feedback loops around the DPC ensure constant gain across supply voltages, reduce distortion, and increase immunity to power supply injected noise and distortion. The analog gain is also applied in the Class-D amplifier section of the device.

The switching rate of the amplifier is internally fixed around 360 kHz.

数字信号经过数字限幅器后，进入了闭环 D 类功放。D 类功放的第一级是数字转 PWM 模块（DPC），PWM 信号则被用来驱动功放输出级。DPC 的反馈环可保证恒定的增益，降低失真，提高对电源噪声的免疫力。该 D 类功放的模拟增益（GAIN_A）可通过寄存器修改。

D 类功放的开关频率被固定在 360kHz 附近。

3 Speaker Amplifier Protection Suite

The speaker amplifier in the HT566 includes a robust suite of error handling and protection features. It is protected against Over-Current, Under-Voltage, Over-Voltage, Over-Temperature, DC, and Clock Errors. The status of some errors is reported via the FAULT pin or/and the appropriate error status register in the I²C Control Port. Table3 details the types of errors protected by the HT566 Protection Suite and how each are handled.

HT566 具有多种保护功能，包括过流、欠压、过压、过温、DC、时钟错误等保护。某些故障将通过\FAULT 引脚和/或寄存器错误标志位反应。下表对这些故障和保护进行了详细说明。

Table3 Protection Suite Error Handling Summary

ERROR	CAUSE	Reported Method	The device resumes normal operation
Overvoltage Error (OVE)	PVDD level rises above that specified by OVE_{RTH}	none	Immediately after PVDD level returning below OVE_{FTH}
Undervoltage Error (UVE)	PVDD level drops below that specified by UVE_{RTH}	none	Immediately after PVDD level returning above UVE_{RTH}
Clock Error (CLKE)	One or more of the following errors has occurred: 1. Non-supported MCLK to LRCK and/or SCLK to LRCK Ratio; 2. Non-supported MCLK or LRCK rate 3. MCLK, SCLK, or LRCK has stopped	\FAULT and Register	Immediately after Clocks returning to valid state
Overcurrent Error (OCE)	Speaker Amplifier output current has increased above the level specified by OCE_{TH}	\FAULT	T_{fault} after \FAULT pin is pulled low
DC Detect Error (DCE)	DC offset voltage on the speaker amplifier output has increased above the level specified by the DCE_{TH}	\FAULT	T_{fault} after \FAULT pin is pulled low
Overtemperature Error (OTE)	The temperature of the die has increased above the level specified by the OTE_{TH}	\FAULT	T_{fault} after \FAULT pin is pulled low

3.1 \FAULT pin

In both hardware and software Control mode, the \FAULT pin of the HT566 serves as a fault indicator to notify the system that a fault has occurred with the device by being actively pulled LOW. This pin is an open-drain output pin and, unless one is provided internal to the receiver, requires an external pullup to set the net to a known value. The behavior of this pin varies based upon the type of error which has occurred.

在硬件工作模式和软件控制模式，HT566 的\FAULT 脚作为故障显示，当芯片发生故障时，该引脚拉低。该引脚是开漏结构的输出脚，需要在外部通过电阻上拉至固定电平，或连接至主控 I/O。

3.2 Over-Current Protection

The HT566 features over-current conditions against the output stage short-circuit conditions. The short circuit protection fault is reported on the \FAULT pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is triggered. The device will automatically attempt to resume after Tfault. If the over-current condition is still not cleared, the device will again go into protection.

HT566 输出级短路时，发生了过流，此时芯片进入保护状态，\FAULT 引脚拉低，功放输出切换到高阻状态。经过 t_{FAULT} 时间后，芯片将自动尝试恢复，若过流状态已消失，芯片恢复；若过流状态仍在，芯片再次进入保护状态。

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3.3 Over-temperature Protection

Over-temperature protection on the HT566 device prevents damage to the device when the internal die temperature exceeds 150°C. This triggering point has a ±15°C tolerance from device to device. Once the die temperature exceeds the thermal triggering point, the device is switched to the shutdown state and the outputs are disabled. Thermal protection faults are reported on the \FAULT pin. The device will automatically attempt to resume after Tfault. If the over-temperature condition is still not cleared, the device will again go into protection.

过温保护在芯片内部结温达到 150℃时发生，以防止芯片损坏，此时芯片进入关断状态，\FAULT 脚拉低。经过 t_{FAULT} 时间后，芯片将自动尝试恢复，若过温状态已消失，芯片恢复；若过温状态仍在，芯片再次进入保护状态。

3.4 Over-voltage Protection

The HT566 device monitors the voltage on PVDD voltage threshold. When the voltage on PVDD pin exceeds the over-voltage threshold (18 V typ), the OVP circuit puts the device into shutdown mode. The device recovers automatically once the over-voltage condition has been removed.

当 PVDD 电压高于过压保护点（OVE_{RTH}）18V 时，芯片进入保护状态，芯片关闭。当 PVDD 低于过压保护点（OVE_{FTH}）后，芯片立即自动恢复。

3.5 Under-voltage Protection

When the voltage on PVDD pin falls below the under-voltage threshold (4.2 V typ), the UVP circuit puts the device into shutdown mode. The device recovers automatically once the under-voltage condition has been removed.

当 PVDD 电压低于欠压保护点（UVE_{FTH}）4.2V 时，芯片进入保护状态，芯片关闭。当 PVDD 高于欠压保护点（UVE_{RTH}）后，芯片立即自动恢复。

3.6 Clock error detection

When any clock of MCLK, SCLK, LRCK halt or shifted to a non-supported speed, the device reports Clock Error in bit [1:0] of Register 0x17 and \Fault pin. The device recovers automatically once the clock-error condition has been removed.

当 MCLK、SCLK、LRCK 停止或为不支持的速率时，芯片进入保护状态，\FAULT 脚拉低，寄存器 0x17 的 bit[1:0]标志位进行相应显示。当故障撤销时，芯片立即自动恢复，\FAULT 恢复高，寄存器标志位恢复。

3.7 DC Detect Protection

The HT566 has circuitry which will protect the speakers from DC current which might occur due to an internal amplifier error. A DC detect fault is reported on the \FAULT pin as a low state. The DC Detect fault also causes the amplifier to shutdown by changing the state of the outputs to Hi-Z. The device will automatically attempt to resume after Tfault. If the over DC current condition is still not cleared, the device will again go into protection.

A DC Detect Fault is issued when the output DC voltage sustain for more than 420 msec at the same polarity. This feature protects the speaker from large DC currents or AC currents less than 2 Hz. To avoid nuisance faults due to the DC detect circuit, hold the \SD pin low at power-up until the signals at the inputs are stable.

HT566 具有 DC 直流保护，以保护扬声器。芯片产生直流保护时，\FAULT 拉低，功放输出切换到高阻状态。经过 t_{FAULT} 时间后，芯片将自动尝试恢复，若故障已消失，芯片恢复；若故障仍在，芯片再次进入保护状态。

当功放输出直流在相同极性保持 420ms 以上时，DC 直流保护触发。

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4 Device Functional Modes

4.1 Software Control and Hardware Control

The HT566 device can be configured via an I²C communication port which is software control mode. Once all powers (PVDD, AVDD, DVDD) are brought up and stable, the device is ready for software control. Before the device is configured into operation (that is bring \SD pin to high, or write Bit "SD" into 1), configure the device via I²C in the manner required by the use case, e.g., bit "PBTL" and "Format".

For systems which do not require the added flexibility of the I²C control port or do not have an I²C host controller, the HT566 can be used directly in Hardware Control Mode with default configurations. The only external I/O that can be controlled in Hardware Control Mode is the \SD pin.

HT566 可以通过 I²C 通讯端口进行配置，即软件控制模式。当 PVDD、AVDD、DVDD 已稳定，芯片的软件控制模式即已准备就绪。在芯片进入工作状态（即将\SD 脚拉高，或将 Bit "SD" 写 1）前，需要通过 I²C 将芯片配置成需要的状态（如 bit "PBTL", "Format"等）。

对于不需要灵活的配置，或没有 I²C 主机的应用，HT566 可工作在硬件模式，此时芯片工作在默认配置，外部唯一可控制的端口即为\SD。

4.2 Speaker Amplifier Shut Down (\SD pin)

The \SD pin is provided to place the speaker amplifier into shutdown. Driving this pin LOW will place the device into shutdown, while pulling it HIGH will bring the device into operation. The shutdown mode is the lowest power consumption mode that the device can be placed in while the power supplies are up.

However, when \SD pin is pulled low, the software control mode is ready, the device is still capable of being configured through I²C port. If the \SD pin is pulled low, and bit SD is written into 1, the device is in operation mode. See as the following table.

\SD 脚拉低时，芯片进入关断模式；\SD 拉高时，芯片进入工作状态。在关断模式下，芯片进入低功耗状态。

需要注意的是，\SD 拉低时，芯片的软件控制模式仍处于准备就绪状态，芯片仍可通过 I²C 控制，此时若将 Bit SD 写 1，芯片仍可进入工作状态。如下表。

Table4 \SD pin and Bit SD

\SD pin	Bit SD	Mode
LOW	1	Normal operation
LOW	0	Shutdown mode
High	0	Normal operation
High	1	Normal operation

4.3 Spread Spectrum and De-Phase

The HT566 device has built-in spread spectrum control of the oscillator frequency and de-phase of the PWM output to improve EMI performance. The spread spectrum scheme is turned on as default, and can be turned off in bit 6:4 of Register 0x19.

De-phase inverts the phase of the output PWM such that the idle output PWM waveforms of the two audio channels are inverted. De-phase does not affect the audio signal, or its polarity. De-phase only works with BD mode; it is auto-disabled in 1SPW mode.

HT566 具有扩频功能，其可通过控制振荡器频率和 PWM 输出保持反向，来抑制 EMI 辐射。扩频功能默认是开启的，其可通过寄存器 0x19 的 bit 6:4 关闭。

PWM 输出保持反向，即在静态下，功放输出的两个通道的 PWM 波形保持反向，其并不影响音频信号，其尽在 BD 模式下有效，1SPW 模式下自动关闭。

4.4 Speaker Amplifier Operating Modes

The HT566 device can be used with two different amplifier configurations, can be configured by Bit 3 of Register 0x18: BTL Mode and PBTL Mode.

In BTL mode, the HT566 amplifies two independent signals, which represent the left and right portions of a stereo signal. The amplified left signal is presented on differential output pair shown as OUTL+ and OUTL-, the amplified right signal is presented on differential output pair shown as OUTR+ and OUTR-.

The PBTL mode of operation is used to describe operation in which the two outputs of the device are placed in parallel to increase the power sourcing capabilities of the device. In this mode, connect the OUTR+ and OUTR- together for the positive speaker terminal and OUTL+ and OUTL- together for the negative speaker terminal. On the input side of the HT566 device, the input signal to the PBTL amplifier is left frame of I²S or TDM data (changeable in bit 7 of register 0x17).

HT566 可通过寄存器 0x18 的 Bit 3 设置 BTL 模式和 PBTL 模式。

在 BTL 模式，HT566 将立体声的两个声道的信号独立放大。左声道信号放大后在 OUTL+和 OUTL-端输出，右声道信号放大后 OUTR+和 OUTR-端输出。

在 PBTL 模式，为了增强输出驱动能力，可将 OUTR+和 OUTR-并联驱动喇叭正端，OUTL+和 OUTL-并联驱动喇叭负端，此时，音频输入的左通道信号将被放大（但可通过寄存器 0x17 的 bit7 调整）。

4.5 Class D Amplifier Modulation

The HT566 device can be used with two different Class D amplifier modulations, can be configured by Bit 7 of Register 0x19.

4.5.1 BD Modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTx+ and OUTx- are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTx+ is greater than 50% and OUTx- is less than 50% for positive output voltages. The duty cycle of OUTx+ is less than 50% and OUTx- is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I²R losses in the load.

HT566 的 D 类功放具有两种调制方式，其可通过寄存器 0x19 的 Bit 7 设置。

这种调制模式使得在功放驱动感性喇叭（较短的喇叭线长）时不需要 LC 滤波器。每个输出在 0V 和 PVDD 间切换，无输入时，OUTx+ 和 OUTx-保持相位一致，以减小流过负载的电流。对于正的输出信号，OUTx+占空比大于 50%，OUTx-占空比小于 50%；对于负的输出信号则相反。

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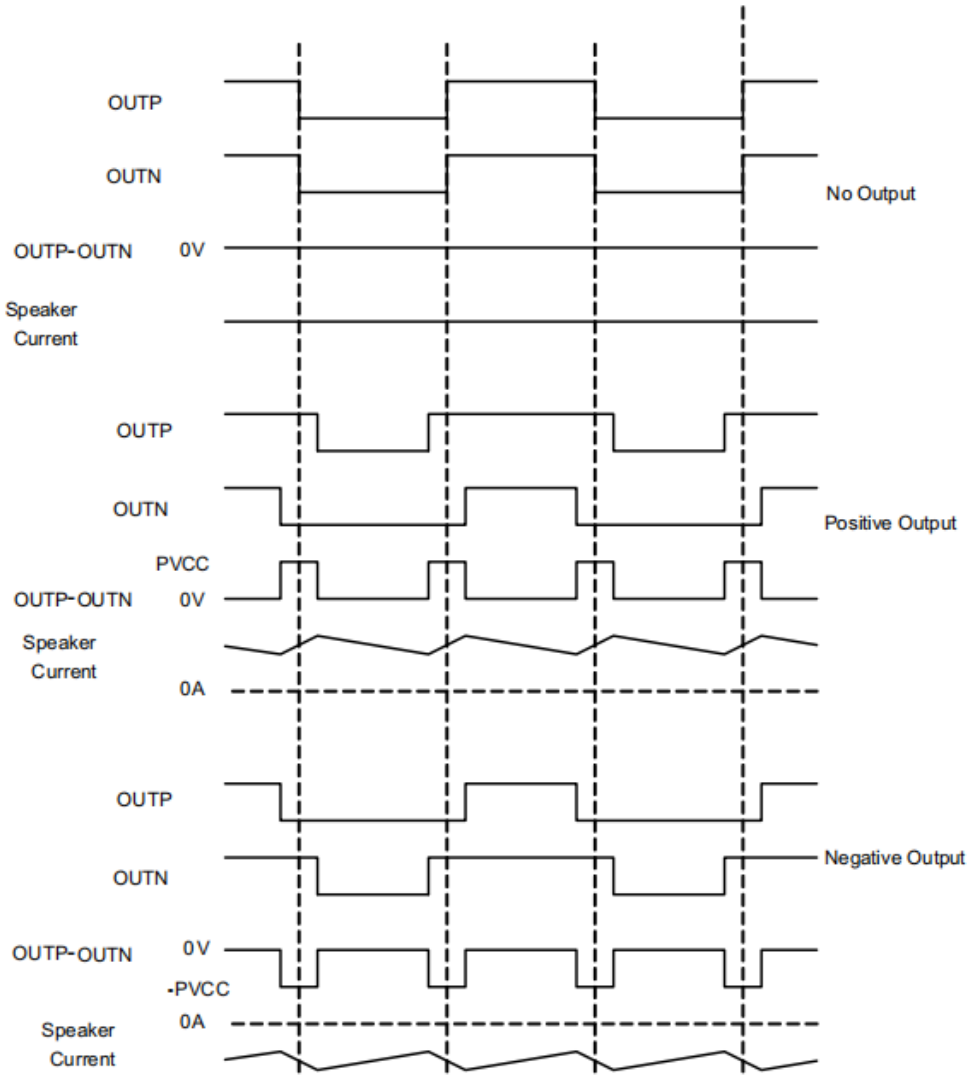

Figure 7 BD Modulation

4.5.2 Low-Idle-Current 1SPW Modulation

The 1SPW mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In 1SPW mode the outputs operate at ~15% modulation during idle conditions. When an audio signal is applied one output decreases and the other output increases. The decreasing output signal rails to GND. At which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses.

1SPW 模式改变了传统的调制方式，以获得更高的效率，同时在 THD 方面有轻微的变差，并且在输出滤波器的选择上需要更多的注意。在静态下，输出开关占空比约 15%。当有信号时，输出一端占空比增加，另一端占空比减小。占空比减小的输出信号端大多数时候即为地电位，此时所有的音频调制发生通过另外一个输出端，结果是在音频周期的大部分时间内，只有一个输出是切换的。由于降低了开关损耗，这种模式的效率得到了提高。

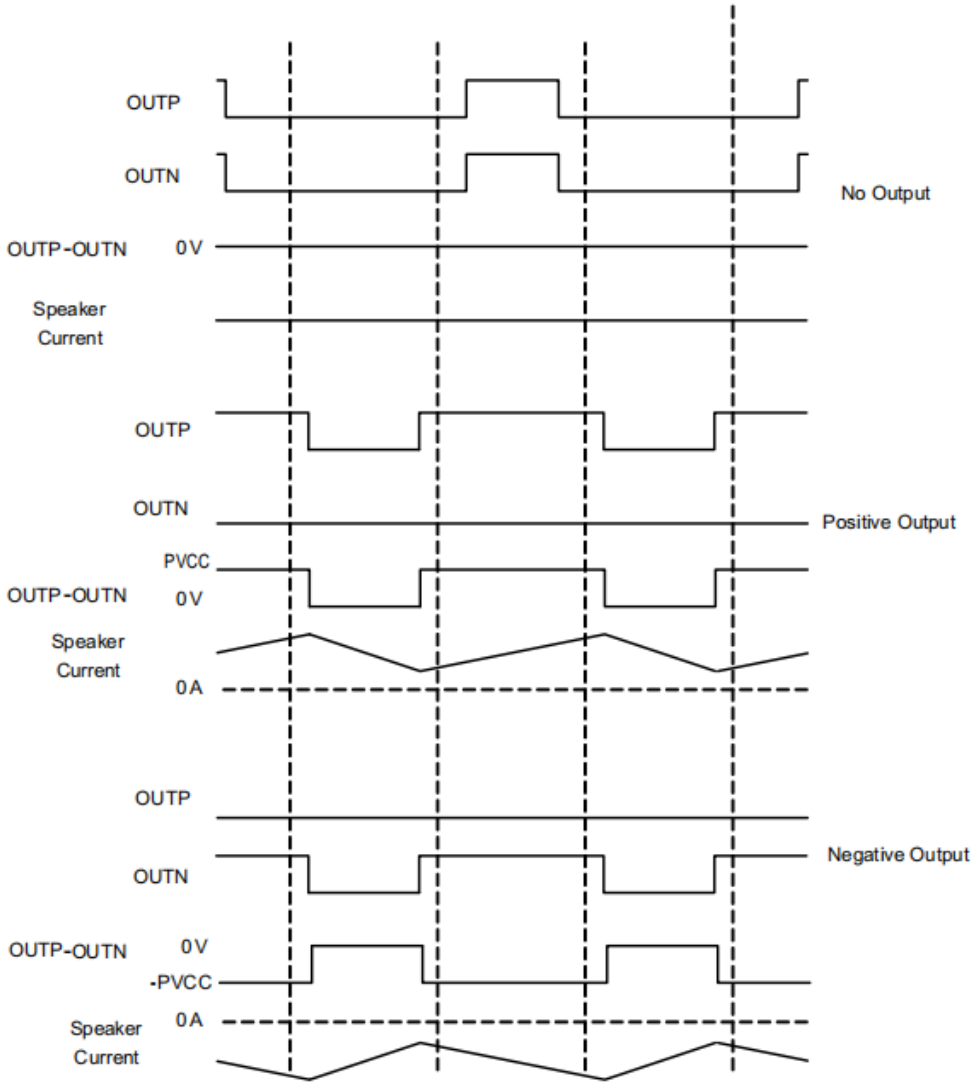

Figure 8 1SPW Modulation

4.6 I²C Control Port

4.6.1 I²C Device Address

Each device on the I²C bus has a unique address that allows it to appropriately transmit and receive data to and from the I²C master controller. As part of the I²C protocol, the I²C master broadcast an 8-bit word on the bus that contains a 7-bit device address in the upper 7 bits and a read or write bit for the LSB. The HT566 has a configurable I²C address. The ADR[1:0] can be used to set the device address of the HT566. The I²C device address is configured as "11011xx [R/W]", where "xx" corresponds to the state of the ADR[1:0] pin at first power up sequence of the device. [R/W] represents 1 when writing, [R/W] represents 0 when reading.

每个器件在 I²C 总线上具有一个独一无二的器件地址，以便正确的将数据传输至 I²C 主机及从 I²C 主机接收数据。作为 I²C 协议的一部分，I²C 主机在总线上广播一个 8 位字节，该字节包含高 7 位的 7 位设备地址和 LSB 的读或写位。HT566 通过引脚 ADR[1:0]可设置 I²C 地址。I²C 地址即为 11011xx [R/W]，其中"xx" 表示上电时引脚 ADR[1:0]的状态，当进行读操作时[R/W]代表 0，当进行写操作时[R/W]代表 1。

Table5 I²C Address Configuration

ADR[1:0]	IIC Address for Reading	IIC Address for Writing
LL	0xD8	0xD9
LH	0xDA	0xDB
HL	0xDC	0xDD
HH	0xDE	0xDF

4.6.2 General Operation of the I²C Control Port

The HT566 device has a bidirectional I²C interface that is compatible with the Inter IC (I²C) bus protocol and supports both 100-kHz and 400-kHz data transfer rates. This is a slave-only device that does not support a multi-master bus environment or wait-state insertion.

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system using serial data transmission. The address and data 8-bit bytes are transferred most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period.

The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bi-directional bus using a wired-AND connection.

Use external pull-up resistors for the SDA and SCL signals to set the logic-high level for the bus.

HT566 I²C 接口支持双向传输，该接口与 I²C 总线协议兼容，并支持 100 kHz 和 400 kHz 数据传输速率。这是一个从设备，不支持多主机的总线环境，及等待状态下的插入。

I²C 总线具有两个信号，SDA（数据）和 SCL（时钟），在系统中的器件之间使用串行数据传输进行通信。地址和数据的 8 位字节首先传输最高有效位（MSB）。此外，总线上传输的每个字节由接收设备用确认位（ACK）进行确认。每个传输操作从主设备驱动总线上的启动条件开始，并以主设备驱动总线上的停止条件结束。当时钟处于逻辑高电平时，总线使用数据终端（SDA）上的转换来指示启动和停止条件。SDA 上的高到低转换表示开始，低到高转换表示停止。正常的数据位转换必须在时钟为低时发生。

主机生成 7 位从机地址和读/写（R/W）位，以打开与另一个设备的通信，然后等待确认条件。在应答时钟周期内，设备保持 SDA 低，以指示确认。当发生这种情况时，主机发送序列的下一个字节。每个设备有唯一的 7 位从机地址加上 R/W 位（1 字节）。所有兼容设备通过并联的总线共享信息。

SDA 和 SCL 需通过外部上拉电阻截至逻辑高电平。

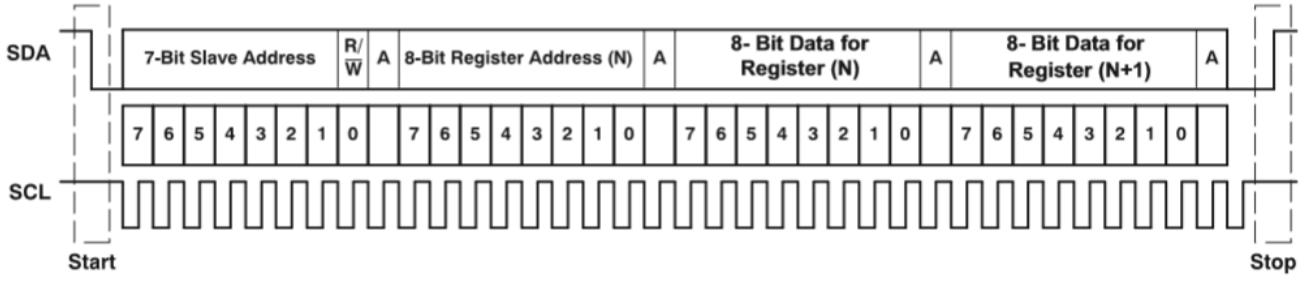

Figure 9 Typical I²C Sequence

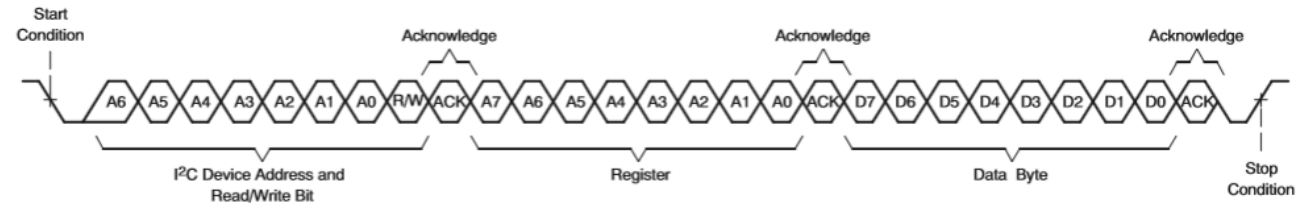

Figure 10 Single-Byte Write Transfer

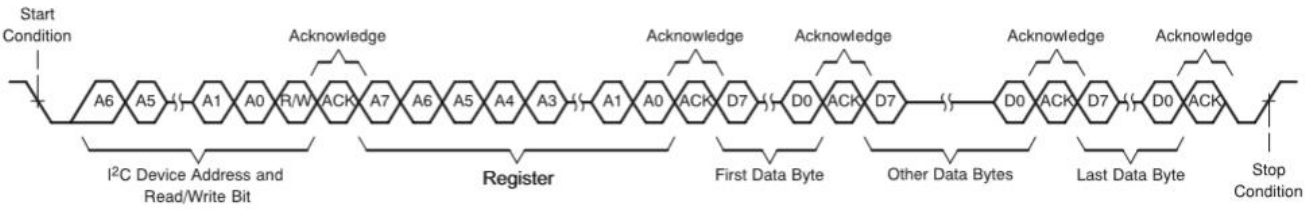

Figure 11 Multiple-Byte Write Transfer

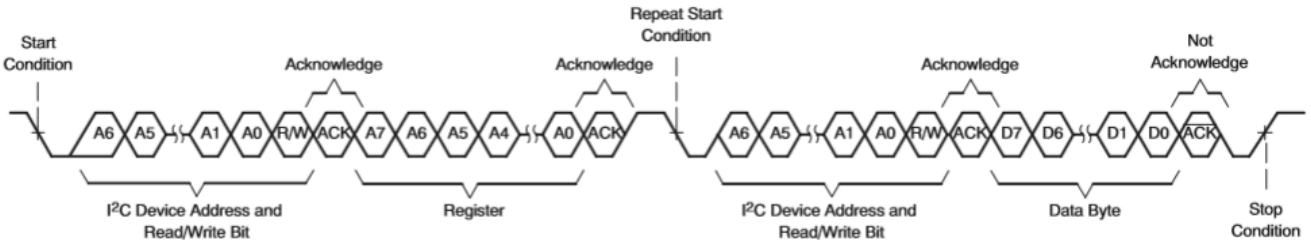

Figure 12 Single-Byte Read Transfer

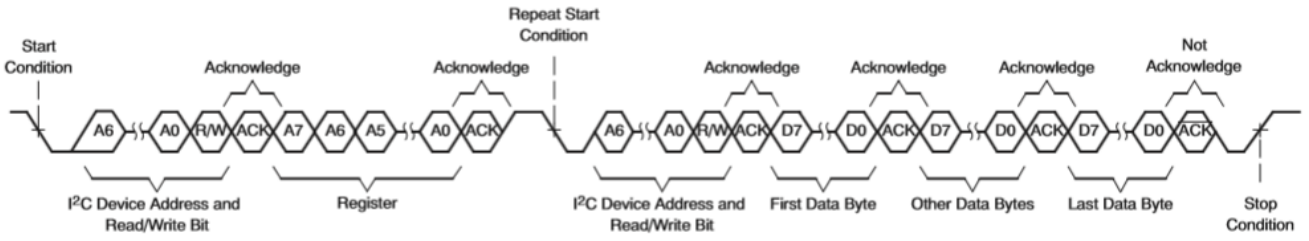

Figure 13 Multiple-Byte Read Transfer

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5 Register Map

Table6 Register Map

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
0x10	Digital Clipper Level DigClip[19:12]								FFh
0x11	Digital Clipper Level DigClip[11:4]								FFh
0x12	Digital Clipper Level DigClip[3:0]				SLEEP	SD	MUTE_A	SPEED	F0h
0x13	Data Format		Word_Length		TDM_Offset	TDM_Slot			00h
0x14	HPF Byps	Left_Mix	Right_Mix	Fade	MUTE_L	MUTE_R	Digital Boost		90h
0x15	Left channel volume control								CFh
0x16	Right channel volume control								CFh
0x17	ch_Shift	Fade_Mode	SCLK_DET_EN	CLK_DET_EN	Reserved		CLK_Error	SCLK_Error	33h
0x18	Reserved	Analog Gain			PBTL	Reserved			02h
0x19	Modulation	Spread Spectrum			Reserved			Gain_Group	70h

The register details are as follows. The blue fonts are the default settings when powering on.

寄存器详细信息如下。蓝色字体为上电时的默认设置状态。

Register Address: 0x10 (default FFh)

Bit	R/W	Label	Default	Description
7:0	R/W	DigClip[19:12]	FFh	The digital clipper level is decoded from 3 registers: DigClip[19:12], DigClip[11:4] and DigClip[3:0]. The default value is the highest value of the level.

Register Address: 0x11 (default FFh)

Bit	R/W	Label	Default	Description
7:0	R/W	DigClip[11:4]	FFh	The digital clipper level is decoded from 3 registers: DigClip[19:12], DigClip[11:4] and DigClip[3:0]. The default value is the highest value of the level.

The digital clipper level determined by DigClip[19:0] is the maximum output threshold level from DAC transferring to the analog Amplifier. The default value of the digital clipper level is the full scale of DAC output, and decreasing the value of DigClip[19:0] will decrease the digital clipper level as well.

Register Address: 0x12 (default F0h)

Bit	R/W	Label	Default	Description
7:4	R/W	DigClip[3:0]	1111	The digital clipper level is decoded from 3 registers: DigClip[19:12], DigClip[11:4] and DigClip[3:0]. The default value is the highest value of the level.
3	R/W	SLEEP	0	0: the device is not in the SLEEP mode; 1: the device is in the SLEEP mode. In sleep mode, the analog Amp is muted, and the digital circuit works with lower current dissipation.
2	R/W	SD	0	0: the device is shut down; 1: the device is not shut down; Notice that if the device is truly shutdown also depends on the \SD pin, see **Speaker Amplifier Shut Down (\SD pin)** .
1	R/W	MUTE_A	0	0: The analog Amp output is not muted 1: The analog Amp output is muted
0	R/W	SPEED	0	0: Serial Audio Port will accept sample rates between 8k – 96kHz 1: Serial Audio Port will accept sample rates between 96kHz-192kHz

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Register Address: 0x13 (default 00h)

Bit	R/W	Label	Default	Description
7:6	R/W	Format	00	Control the Serial Audio Port data format 00: I²S 01 : Left justified 10: Rright justified 11: TDM
5:4	R/W	Word_Length	00	Control the Serial Audio Port sample word length 00: 32bits 01: 24 bits 10: 20bits 11: 16bits
3	R/W	TDM_Offset	0	Control the offset of TDM data in the audio frame. The offset is defined as the number of SCLK from starting (MSB) of audio frame to the starting of the desired audio sample, see Figure 5 TDM Audio Data Format. 0: offset = 0 SCLK 1: offset = 1 SCLK
2:0	R/W	TDM_Slot	000	Control the slot number of TDM data in the audio frame. The slot number is defined as Figure 5 TDM Audio Data Format. 000: Slot0_A + Slot0_B; 001: Slot1_A + Slot1_B; … 111: Slot7_A + Slot7_B;

Register Address: 0x14 (default 90h)

Bit	R/W	Label	Default	Description
7	R/W	HPF Byps	1	0: The internal high-pass filter in the digital path is bypassed 1: The internal high-pass filter in the digital path is not bypassed
6	R/W	Left_Mix	0	0: Left channel mixer is disabled 1: Left channel mixer is enabled, so that left = 1 / 2(left+right)
5	R/W	Right_Mix	0	0: Right channel mixer is disabled 1: Right channel mixer is enabled, so that right = 1 / 2(left+right)
4	R/W	Fade	1	0: Volume fading is disabled; 1: Volume fading is enabled
3	R/W	MUTE_L	0	MUTE the L channel digital output: 0: the left channel is not muted 1: the left channel is muted
2	R/W	MUTE_R	0	MUTE the R channel digital output: 0: the right channel is not muted 1: the right channel is muted
1:0	R/W	Dig Bst	00	Digital Boost setting 00: +0dB is added to the signal in the digital path 01: +6dB is added to the signal in the digital path 10: +12dB is added to the signal in the digital path 11: +18dB is added to the signal in the digital path

Register Address: 0x15 (Default CFh)

Bit	R/W	Label	Default	Description
7:0	R/W	Vol_L	CFh	Left channel Volume control 1111,1111: +24dB; 1111,1110: 23.5dB ……Gain decreased by 0.5dB every step 1100,1111: 0dB ……Gain decreased by 0.5dB every step 0000,0111: -100dB Any setting less than 0000,0111 places the channel in MUTE

Register Address: 0x16 (Default CFh)

Bit	R/W	Label	Default	Description
7:0	R/W	Vol_R	CFh	Left channel Volume control 1111,1111: +24dB; 1111,1110: 23.5dB ……Gain decreased by 0.5dB every step 1100,1111: 0dB ……Gain decreased by 0.5dB every step 0000,0111: -100dB Any setting less than 0000,0111 places the channel in MUTE

Register Address: 0x17 (default 33h)

Bit	R/W	Label	Default	Description
7	R/W	ch_Shift	0	0: The left and right channels are not shifted 1: The left and right channels are shifted
6	R/W	Fade_Mode	0	0: The volume is fading by 0.5dB/8T_{LRCK} 1: The volume is fading by 0.5dB/T_{LRCK}
5	R/W	SCLK_DET_EN	1	SCLK error detection, such as SCLK missing detection, SCLK range detection, SCLK/LRCK detection. If error detection is enabled, once any such error is detected, the relevant error flag will change to 1. 0: SCLK error detection is disabled; 1: SCLK error detection is enabled.
4	R/W	CLK_DET_EN	1	Audio serial port clock error detection, including SCLK, MCLK, LRCK. Once any error such as missing or wrong range of these clocks is detected, the relevant error flag will change to 1. 0: CLOCK error detection is disabled; 1: CLOCK error detection is enabled.
3:2	R	Reserved	00	Unused, make it always 00
1	R	CLK_Error	1	Changes to 0 when Clock Error is detected; back to 1 when Clock Error evacuated;
0	R	SCLK_Error	1	Changes to 0 when SCLK Error is detected; back to 1 when SCLK Error evacuated;

Register Address: 0x18 (Default 02h)

Bit	R/W	Label	Default	Description	
7	R	Reserved	0	Unused, make it always 0	
6:4	R/W	A_GAIN	000	Set analog gain: (Not available yet)	
				000: Gain0 = 19.9dB; Gain1 = 29.3dB	001: Gain0 = 18.7dB; Gan1 = 26.3dB
				010: Gain0 = 17.7dB; Gan1 = 24.1dB	011: Gain0 = 16.9dB; Gan1 = 22.4dB
				100: Gain0 = 16.1dB; Gan1 = 20.9dB	101: Gain0 = 15.3dB; Gan1 = 19.6dB
				110: Gain0 = 14.6dB; Gan1 = 18.5dB	111: Gain0 = 14.0dB; Gan1 = 17.6dB
3	R/W	PBTL	0	0: BTL mode; 1: PBTL mode.	
2:0	R	Reserved	010	Unused, make it always 010	

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Register Address: 0x19 (default 70h)

Bit	R/W	Label	Default	Description
7	R/W	Modulation	0	0: BD mode; 1: 1SPW mode The modulation is only changed when the device is brought from shutdown back into operation after this bit is changed.
6:4	R/W	Spread	111	111: Spread Spectrum on 011: Spread Spectrum off Spread Spectrum function is only switched when the device is brought from shutdown back into operation after this bit is changed.
3:1	R	Reserved	000	Unused, make it always 000
0	R/W	GAIN_Group	0	Select gain group for A_GAIN (Not available yet) (register 0x18, bit [6:4]. 0: Gain0; 1: Gain1 The gain group is only changed when the device is brought from shutdown back into operation after this bit is changed.

6 Typical Applications

6.1 Startup Procedures

1. Configure I/O pins (ADR[1:0]);
2. \SD pin = Low;
3. Bring up power supplies (it does not matter if PVDD, AVDD or DVDD comes up first, provided the device is held in shutdown);
4. Once power supplies are stable, start MCLK, SCLK, LRCK;
5. Configure the device via the control port in the manner required by the use case; especially bit "PBTL", "Format" (as "A" shown in the following figure).
6. Once power supplies and clocks are stable and the control port has been programmed, bring \SD pin High, or write bit "SD" (Bit 2 of Register 0x12) as 1;
7. The device is now in normal operation. Fade in SDIN if needed. The device is still configurable through IIC port. (as "B" shown in the following figure)

The sequence diagram is shown in Figure 14 and Table 7.

1. 通过引脚ADR[1:0]设置器件地址；
2. \SD脚拉低;
3. 接入电源（器件关断状态下，PVDD、AVDD、DVDD上电先后顺序无严格要求);
4. 当电源稳定后，开启MCLK, SCLK, LRCK;
5. 通过IIC进行正确的配置，如“PBTL”，“Format”等（下图中的“A”）;
6. \SD脚拉高，或写bit“SD”为1 (寄存器 0x12的Bit 2);
7. 器件进入正常工作模式。若需要可将SDIN通过渐变引入。此后仍可通过IIC进行部分配置。（下图中的“B”）

具体时序如下图 Figure 14和下表Table 7.

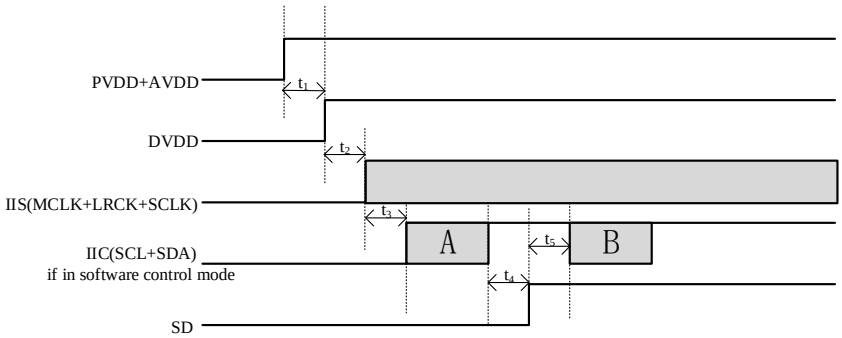


Figure 14 Power-on Sequence

Table 7 Recommendations for Power-on Timing

Symbol	CONDITION	MIN	TYP	MAX	UNIT
t1		0			ms
t2		0			ms
t3		1			ms
t4		1			ms
t5		200			ms

6.2 Power down Procedures

1. The device is in normal operation;
2. Fade out SDIN if needed; The device is configurable through IIC port before power off;
3. Pull \SD pin Low, or write bit “SD” (Bit 2 of Register 0x12) as 0;
4. The clocks can be stopped, and power supplies brought down;
5. The device is now fully shutdown and powered off.

The sequence diagram is shown in Figure 15 and Table8.

芯片处于工作状态;

1. 若需要可将SDIN淡出；器件仍可在关闭之前通过IIC配置；
2. 将\SD脚拉低，或写bit “SD” 为0 (寄存器0x12的Bit 2);
3. MCLK, SCLK, LRCK关闭，然后电源关闭;
4. 芯片已关闭.

具体时序如下图 Figure 15和Table8.

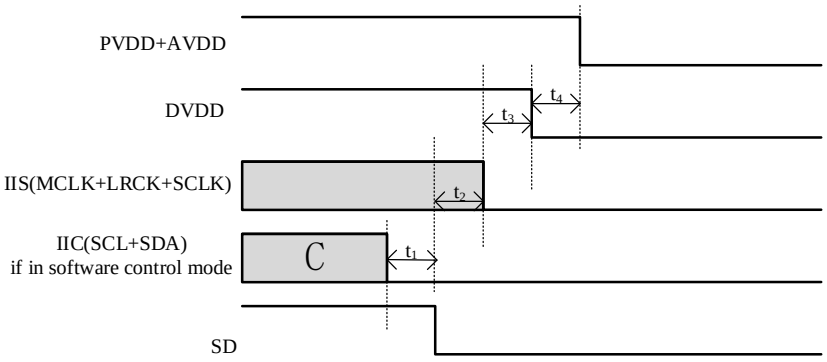
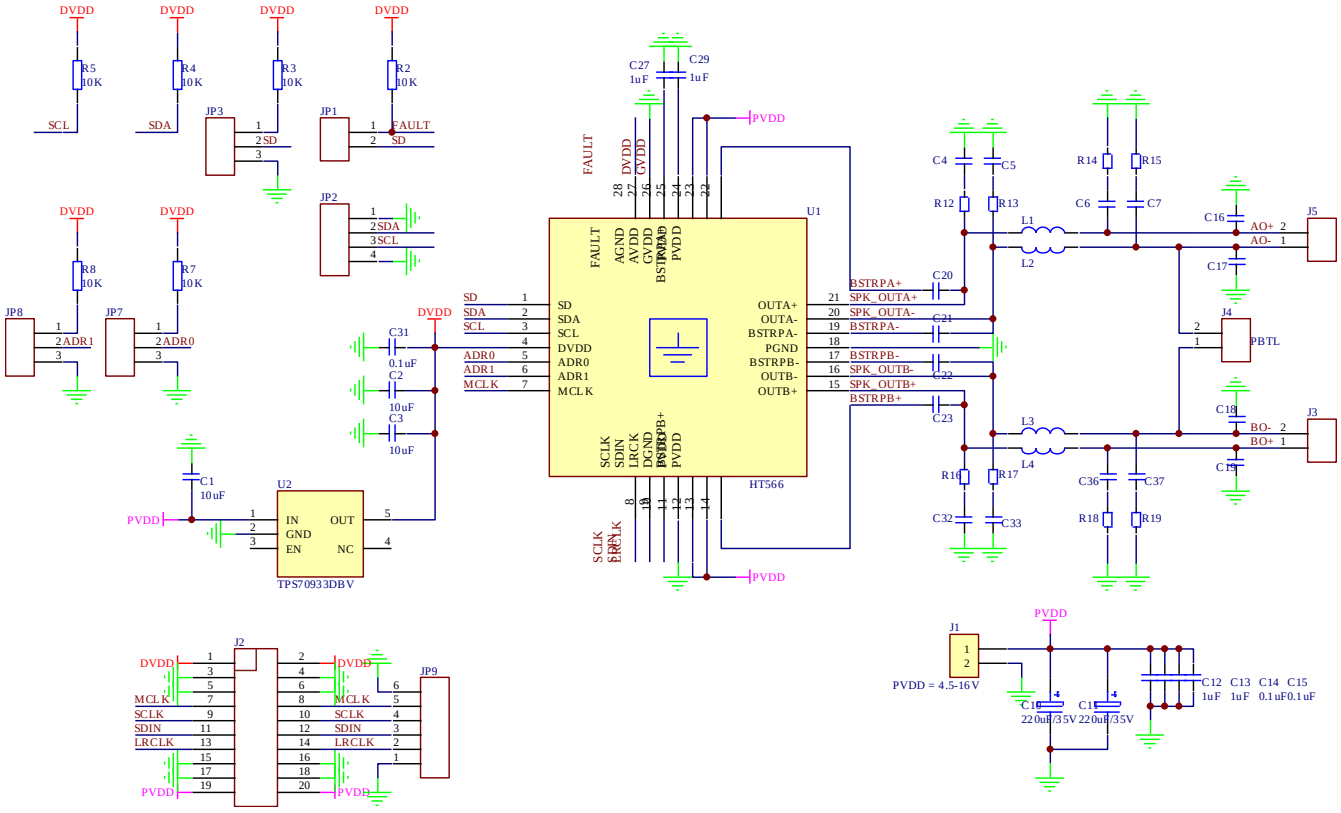


Figure 15 Power-off Sequence

Table8 Recommendations for Power-off Timing

Symbol	CONDITION	MIN	TYP	MAX	UNIT
t_1		1			ms
t_2	Fade-out disabled	1			ms
	Fade-out enable	45			ms
t_3		1			ms
t_4		0			ms

6.3 Typical Circuit Diagram



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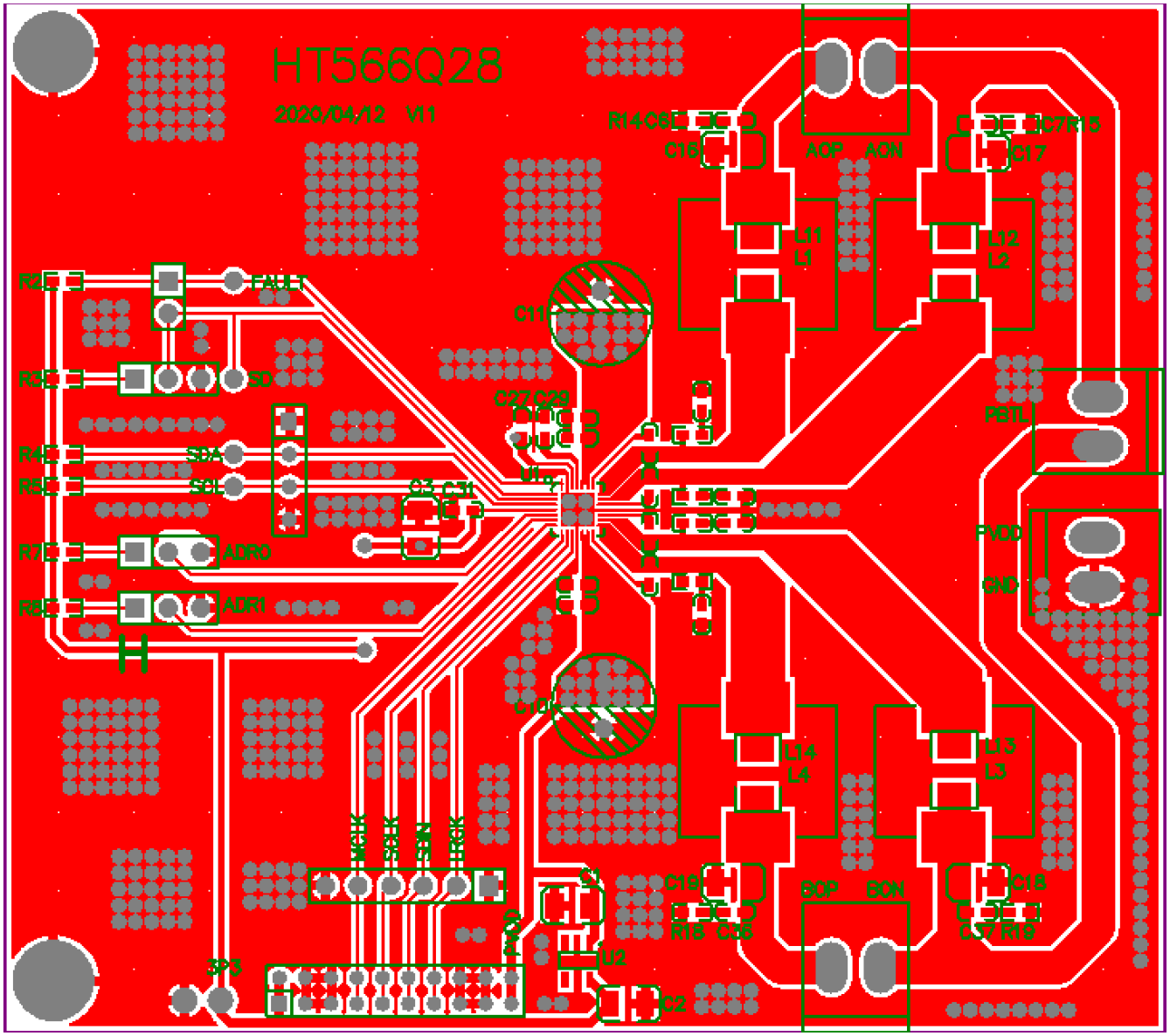
7 PCB Layout

7.1 Top Layer



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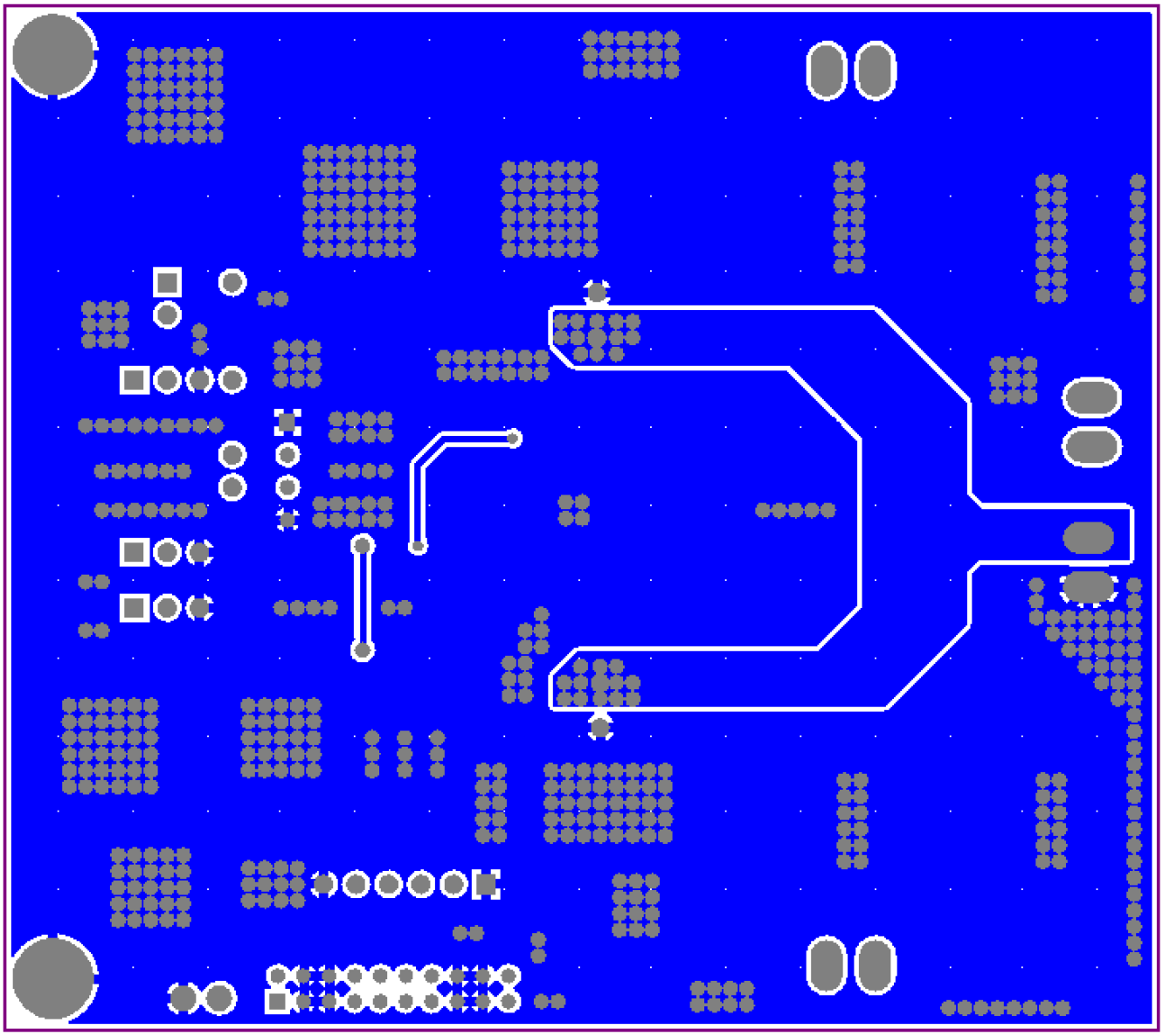
7.2 Bottom Layer



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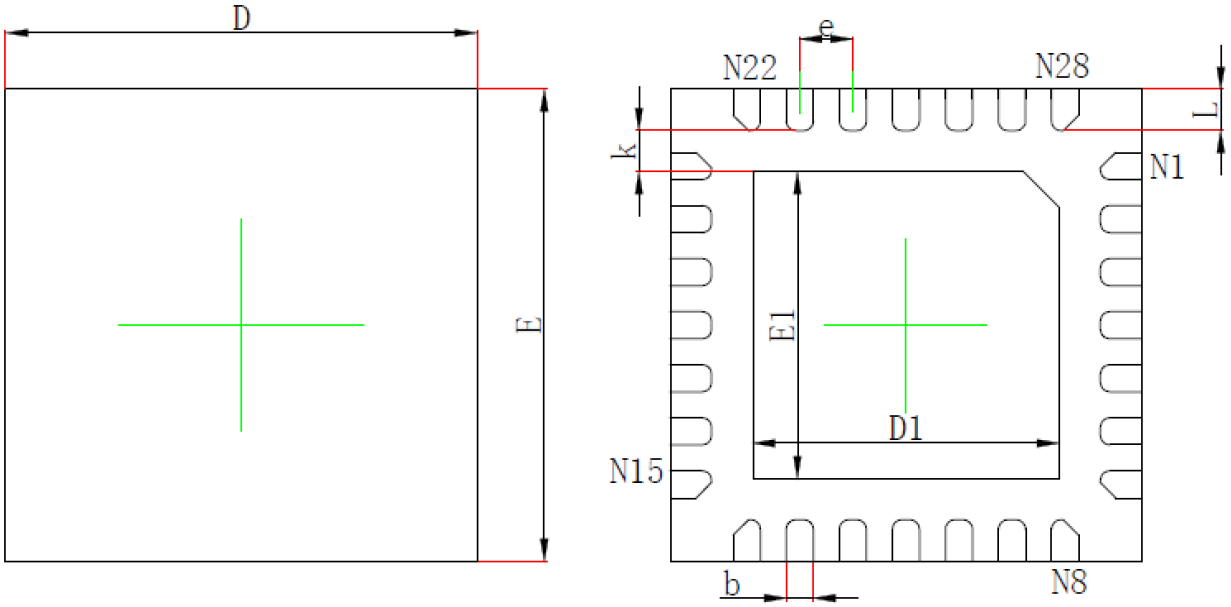
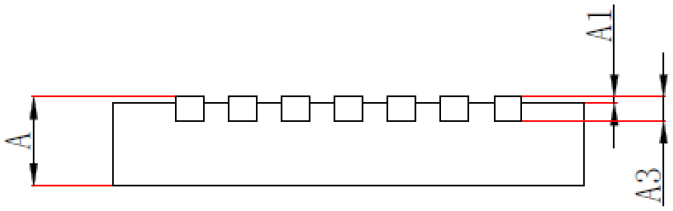
■ PACKAGE OUTLINE



Top View

Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
E1	2.500	2.700	0.098	0.106
D1	2.500	2.700	0.098	0.106
k	0.200MIN		0.008MIN	
b	0.180	0.280	0.007	0.011
e	0.450TYP.		0.018TYP.	
L	0.274	0.426	0.011	0.017